CHIPONE
集创北方

ICND2019

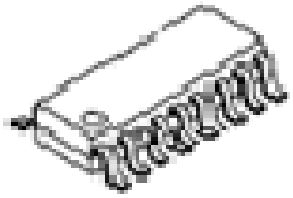
(8-Channel Power Switch for LED Display)

Description

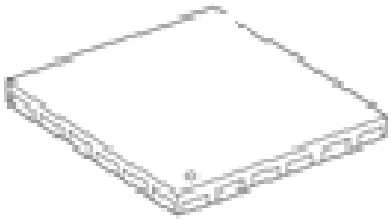
ICND2019 is a 8-channel power switch for LED display.ICND2019 Integrated 74HC595 (8-bit serial-in, serial parallel-out shift register) and 8 Channel N-Channel Enhancement Mode MOSFET driver.

ICND2019 integrated Ghosting Reduction, Caterpillar Cancelling and LED Protection circuit.

AP:SOP



AN：QFN

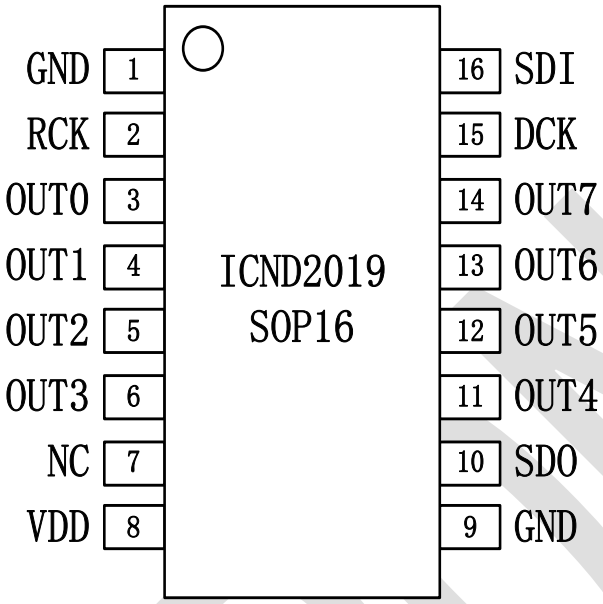


Features

- ✧ Integrated 74HC595 (8-bit serial-in, serial parallel-out shift register)
- ✧ 8 Channel N-Channel Enhancement Mode MOSFET driver
- ✧ N-MOSTEF $R_{ds(ON)}$ 100 mΩ，Max output current 2.5A
- ✧ Ghosting Reduction
- ✧ Caterpillar Removal for LED Short
- ✧ LED Protection
- ✧ Max Power Dissipation <625mW @ VDD=5V & Ivdd=2.5A
- ✧ Up Ghosting Level Adjustable

Pin Configuration

1 AP: SOP16

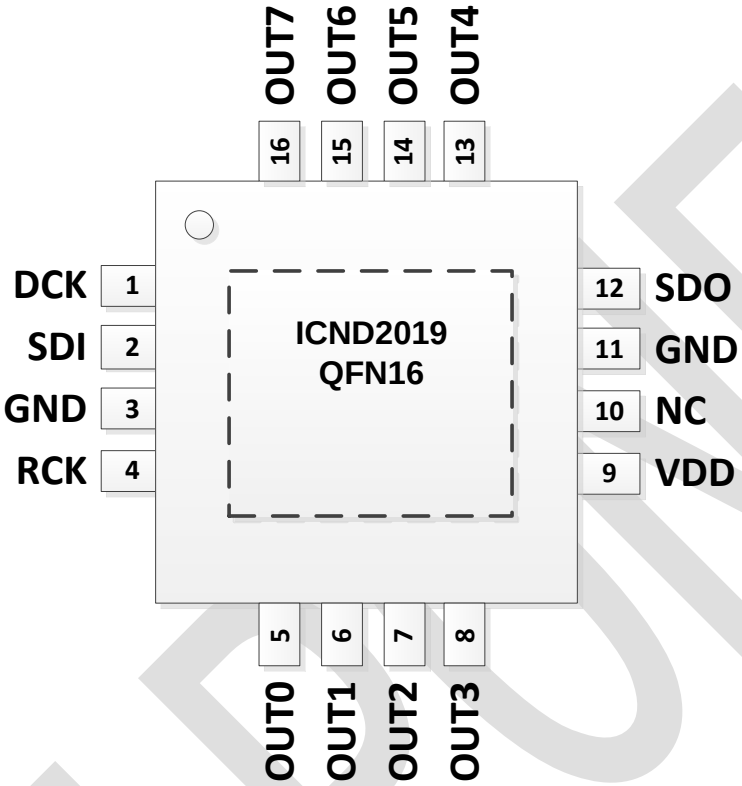


ICND2019AP（SOP16）		
Pin No	**Pin Name**	**Function**
1，9	GND	Power Ground
2	RCK	Register Input
3~6,11~14	OUT0~OUT7	Output with N-Channel Enhancement Mode MOSFET
7	NC	Not Connected
8	VDD	Power-Supply Voltage
10	SDO	Serial Data Output
15	DCK	Shift Clock Input
16	SDI	Serial Data Input

Note:

For control card, SDI is the C of 3-8 decoder, DCK is the A of 3-8 decoder, RCK is the B of 3-8 decoder

2 AN: QFN16



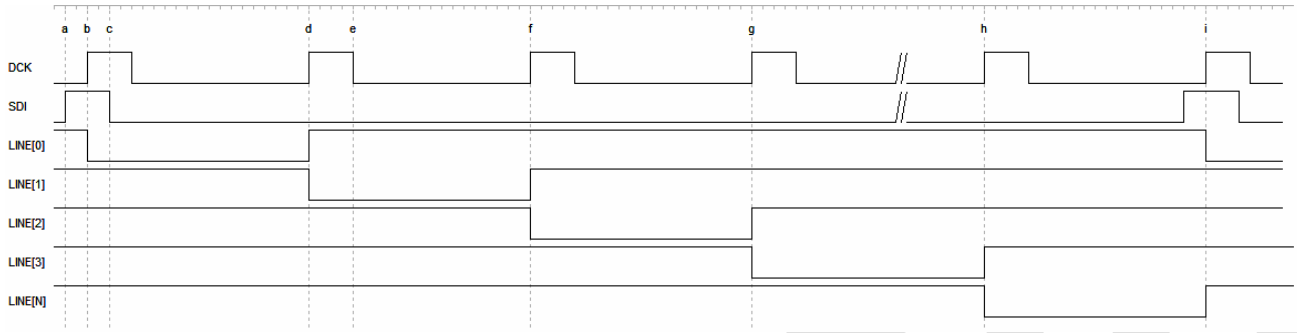
ICND2019AN（QFN16）		
Pin No	**Pin Name**	**Function**
1	DCK	Shift Clock Input
2	SDI	Serial Data Input
3,11	GND	Power Ground
4	RCK	Register Input
5~8, 13~16	OUT0~OUT3, OUT4~OUT7	Output with N-Channel Enhancement Mode MOSFET
9	VDD	Power-Supply Voltage
10	NC	
12	SDO	Serial Data Output

Note:

For control card, SDI is the C of 3-8 decoder, DCK is the A of 3-8 decoder, RCK is the B of 3-8 decoder

Time Waveform

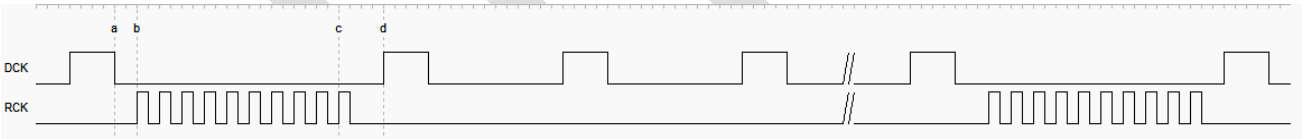
The rising edge of DLK is a line feed signal. After receiving the rising edge of DCLK, the data is shifted once, and the corresponding open channel is also shifted. The width of DCLK is the elimination time, so we need to do DCLK width and interface elimination parameter linkage.



Time	Function	MIN
Tb-Td	***Display time***， between the two DCLK rising edge	
Te-Tf	***Registers configure time*** **,**the DLCK falling edge to the next rising edge	
Td-Te	***Ghost reduction time***, DCLK pulse width	500ns
Ta-Tb	Setup time	20ns
Tb-Tc	Hold time	20ns

Register Setting

Ta-Td，***Registers configure time,*** the DLCK falling edge to the next rising edge.



Register and Number of RCLK Rising Edge when DCK is High.

Reg[3:0]=RCLK-8

Time	Function	MIN
Tb-Tc	Register configuration time（Reg[3:0]=RCLK-8）	
Ta-Tb	Register configuration pre blank area	100ns
Tc-Td	Register configuration behind blank area	100ns

Register

Number of RCK Rising Edge when DCLK is Low	Model<3:2>	Model	Level <1:0>	Level (V)
8	00	1	00	2.5
9			01	2.75
10			10	3.0
11			11	3.25
12	01	2	00	2.5
13			01	2.75
14			10	3.0
15			11	3.25
16	10	3	00	2.5
17			01	2.75
18			10	3.0
19			11	3.25
20	11	0	00	2.5
21			01	2.75
22			10	3.0
23			11	3.25

Default<3:0>=1111

Specifications

Maximum Ratings (T_a =25℃)

Characteristics	Symbol	Rating	Unit
Supply Voltage	VDD	-0.5 ～ +6.0	V
Input Voltage	VIN	-0.5 ～ VDD+0.5	V
Power Dissipation	PD	<625	mW
Operating Temperature	Topt	-40 ～ +80	℃
Storage Temperature	Tstg	-50 ～ +150	℃

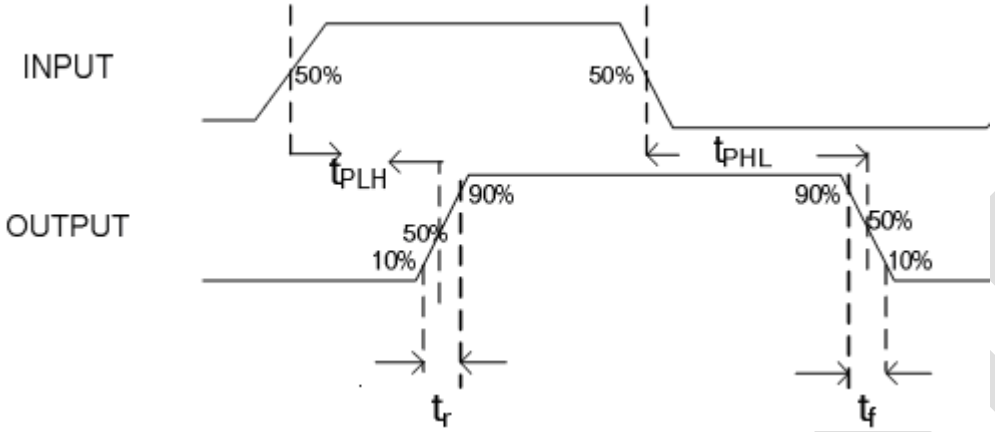
DC Items (Unless otherwise specified, T_a =-40℃~85℃)

Characteristics	Symbol	Min	Typ	Max	Unit	Test Conditions
Power Supply Voltage	VDD	3.0	5.0	5.5	V	-
High Level Logic Input Voltage	VIH	3.0			V	VDD=5.0V
High Level Logic Input Voltage	VIL			2.0	V	VDD=5.0V
Quiescent Device Current	IDD		2.8		mA	VDD=5.0V
Drain Current	IOH			2.5	A	VDD=5.0V
Drain-Source On-State Resistance	RDS(on)		100		mΩ	VDD=5.0V

Switching Characteristics (Unless otherwise specified, T_a =25℃，V_{DD} =5.0V)

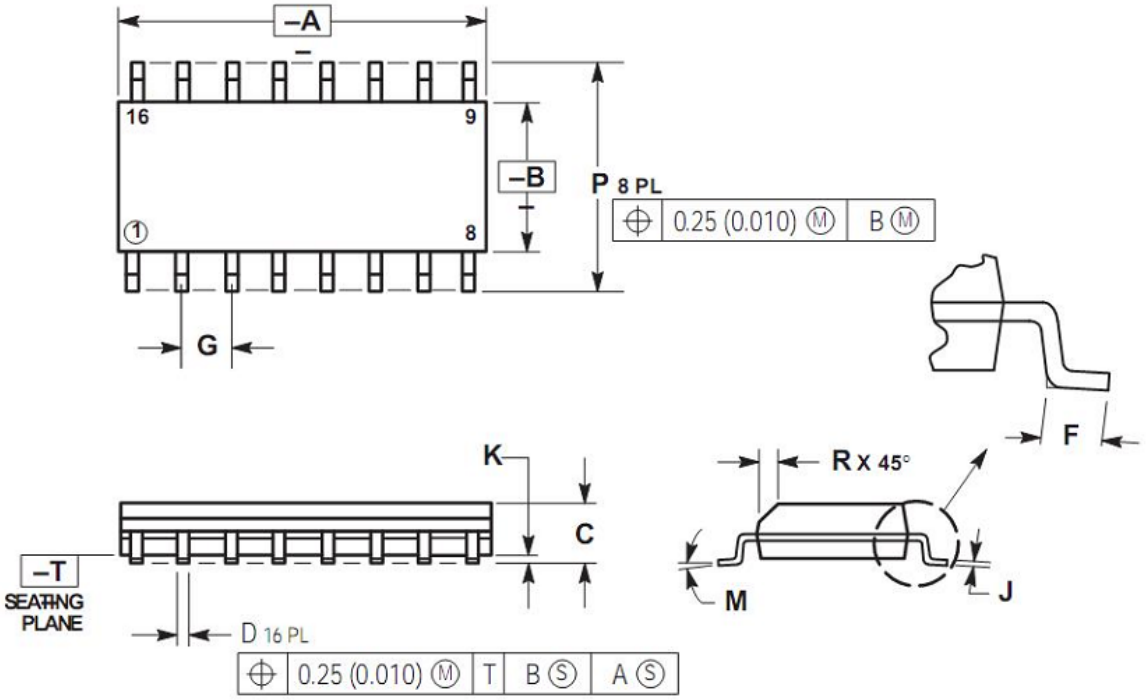
Characteristics	Symbol	Min	Typ	Max	Unit	Test conditions
Propagation	tPLH		95		nS	VDD=5.0V
Delay Time	tPHL		36		nS	CL=2nF
Output rise Time	tr		90		nS	
Output fall Time	tf		62		nS	

Waveform



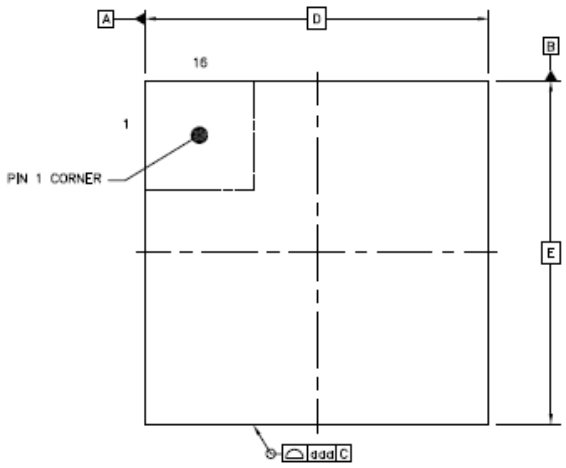
Package Outline

SOP16

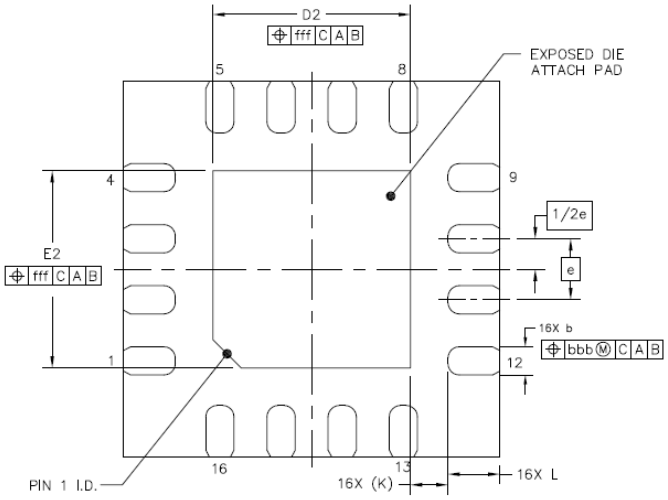


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.224
R	0.25	0.50	0.010	0.019

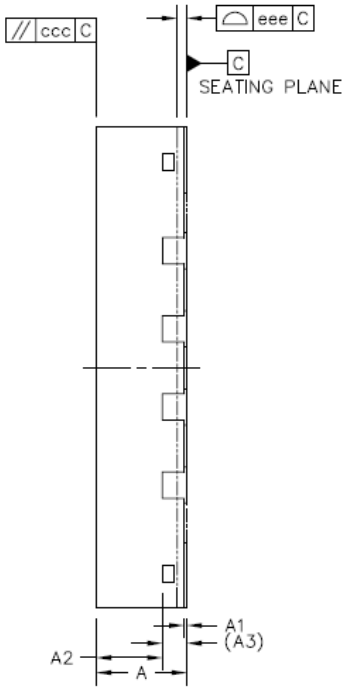
QFN16



TOP VIEW



BOTTOM VIEW



SIDE VIEW

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.25	0.3	0.35
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.65 BSC	
EP SIZE	X	D2	2	2.1	2.2
	Y	E2	2	2.1	2.2
LEAD LENGTH		L	0.45	0.55	0.65
LEAD TIP TO EXPOSED PAD EDGE		K		0.4 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	

Product Ordering Information

Product number	Package （Pb-Free）	Package （mm）	Weight （mg）
ICND2019AP	SOP16	9.9*3.9*1.4	159.5
ICND2019AN	QFN16	4*4*0.75	

Revision History

Rev	Date	Description
1.0	2018/09	Initial Release
1.1	2019/04	Add Register
1.2	2019/05	Add QFN Package

Important information

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