CHIPONE

集创北方

ICND2037S

(16-Channel Constant Current LED Sink Driver with Dual Latch)

Description

The ICND2037S is a 16-channel constant current sink output LED driver. All 16-channels constant current can be set by a single external resistor, which provides users flexibility in controlling the light intensity of LEDs.

The ICND2037S exploits current precision controlling technology , which makes error between ICs less than ±3.5%, and error between channels less than ±3.0%. At ICND2037S output stage , 16-regulated output ports are designed to provide uniform and constant current sinks for driving LEDs within a large range of forward voltage(VF) variations.

ICND2037S contains two 16-bit shift registers and latches which convert serial input data into parallel output format. For integrated dual latches, ICND2037S could get higher refresh rate.

Package

Shrink SOP

SSOP24-150-0.635

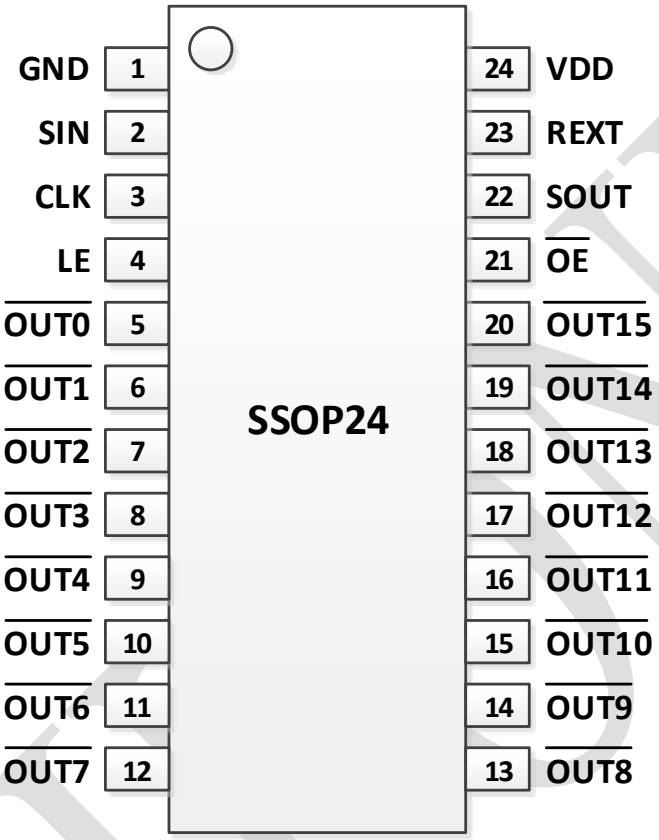
ICND2037S

Features

- 16-channel constant current output
- Output current setting range :
  2~25mA×16@V_{DD}=5V constant current output
  2~20mA×16@V_{DD}=1.2Vconstant current output
- Current accuracy
  Between channel :< ±3.0%
  Between ICs :< ± 3.5%
- Fast response of output current,
  $\overline{OE}$ (min):40ns@V_{DD}=5V
- I/O: Schmitt trigger input
- Data transfer frequency:f_{MAX}=25MHz(Max)
- Power supply voltage: VDD=3.3 ~ 5V
- Operating Temperature: –40°C to +85°C
- Adjustable Pre-Charge for Ghosting Reduction
- LED Protection Circuit
- Integrated Dual Latches for higher refresh rate

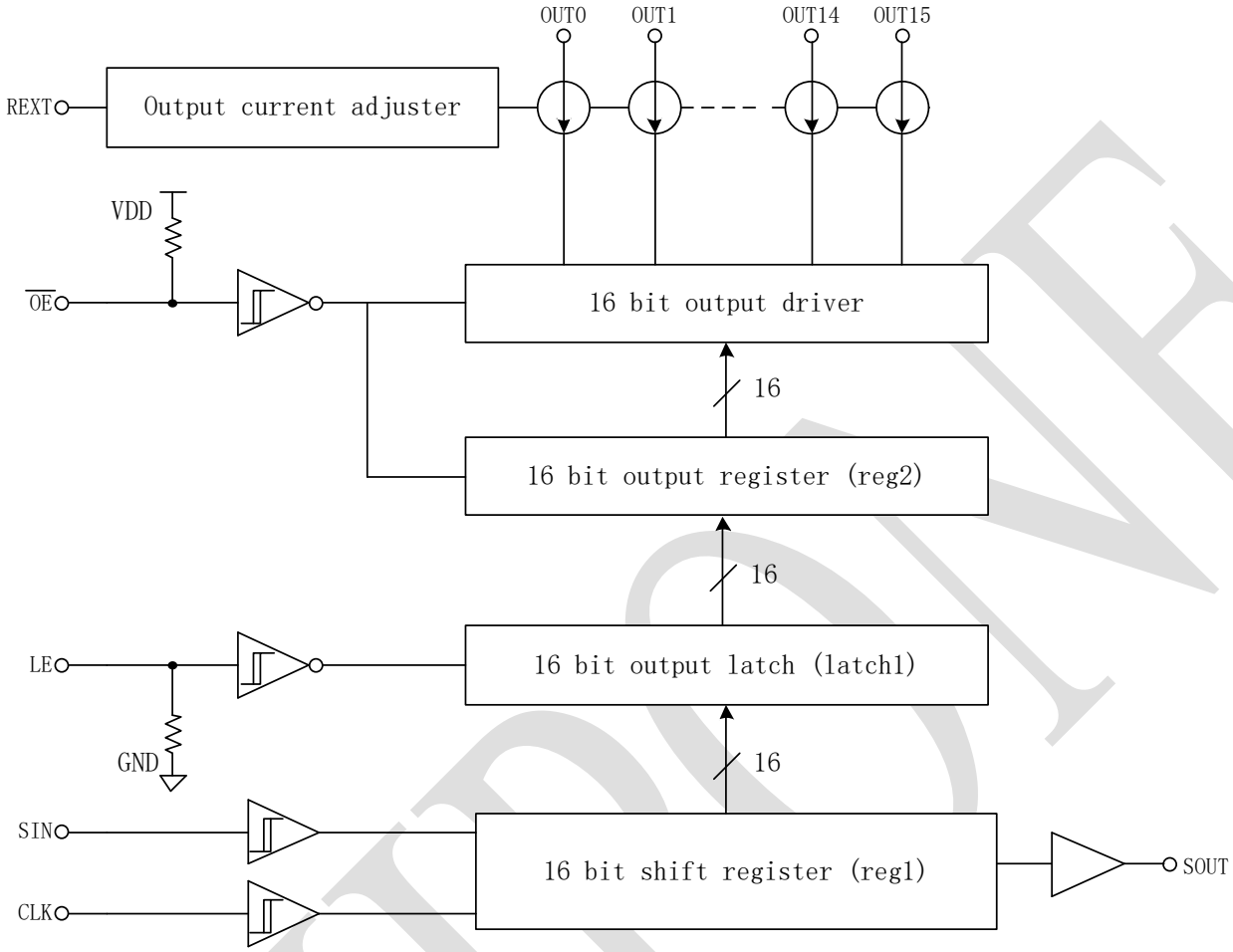
Pin Configuration

SSOP24-P-150-0.635



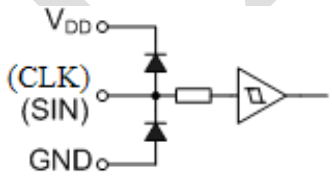
ICND2037S (SSOP24)		
Pin No.	Pin Name	Function
1	GND	Power Ground
2	SIN	Serial data or command input for driver control
3	CLK	Clock input terminal for data shift on rising edge
4	LE	The command parser is a counter of LE length: A different length of LE indicates a different command.
5～20	$\overline{OUT0}$ ~ $\overline{OUT15}$	Constant current output
21	$\overline{OE}$	Output enable terminal, $\overline{OE}$ low level, all output drivers are turned ON ; $\overline{OE}$ high level, all output drivers are turned OFF
22	SOUT	Serial-data or command output to the following IC.
23	R-EXT	Constant-current value setting .Connection to an external resistor to GND.
24	VDD	Power-supply voltage

Block Diagram

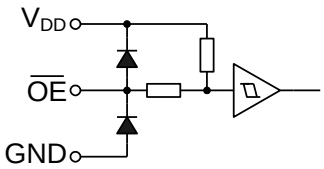


I/O Equivalent Circuits

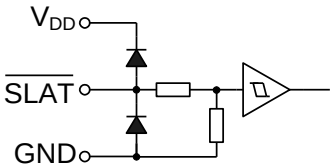
1. CLK, SIN



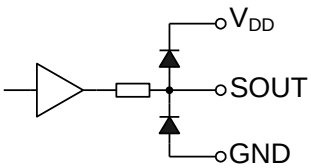
2. $\overline{OE}$



3. LE



4. SOUT



Shift-Register and Command Parser

A simple 16bit shift-register is integrated. All data, such as gray scale and configuration, are latched by the shift-register.

The command parser is a counter of LE length: A different length of LE indicates a different command. Such as a 1bit LE is a “Data Latch” command which indicates that there is a gray scale written in. It will send the 16bit data on shift-register to SRAM.

Control Command

Command Name	Number of DCLK Rising Edge when LE is High	Description
DATA_LATCH	0	Transfer Serial data to buffers(Ghosting Reduction disable)
	1~3	Transfer Serial data to buffers(Ghosting Reduction enable）
--	4~10	Reserved
WR_REG1	11	Write Configuration Register

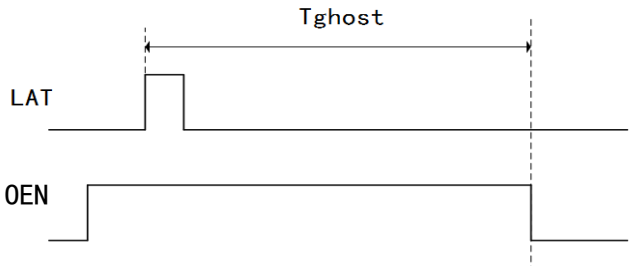
Note1：The length of LE is defined as this: How many positive-edges of DCLK when LE stays logic “1”. For example, the first pulse of LE in the next figure is show a length of 3, which is a “Data Latch” command.

Register

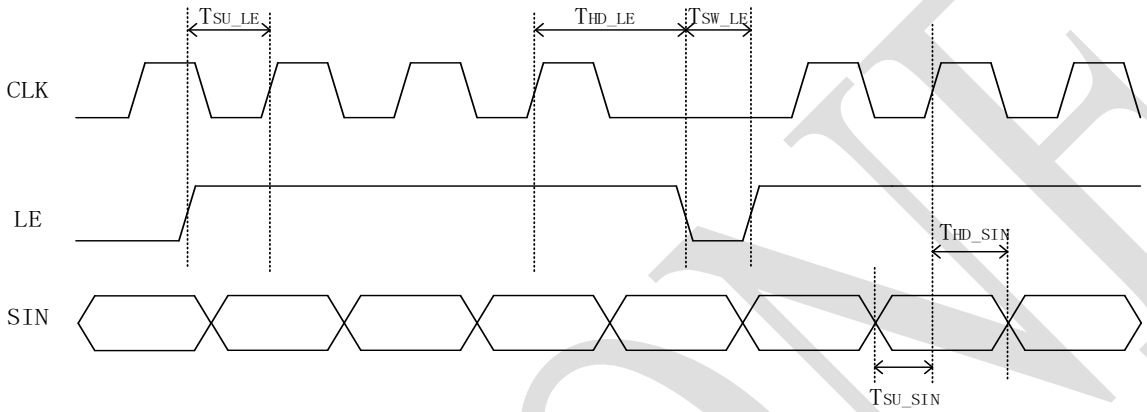
BIT	NAME	Default	Description
15	-	-	Reserved
14:11	R_UP	4'h0	Ghost Reduction Level adjust VR_UP=VDD-2V+ <14:11>*0.1V
10:0	-	-	Reserved

Ghost reduction timing

Tghost means the positive-edge of LAT to the negative-edge of OEN when OEN stays logic “1”.



LE waveforms

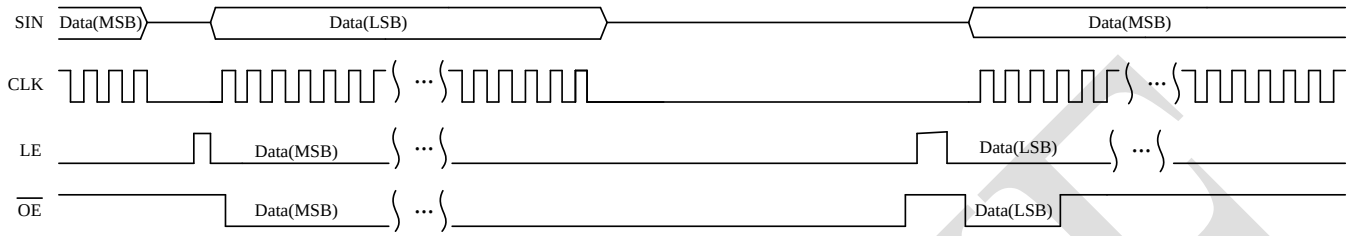


Hold time

Name	MIN	Note
T_{su_LE}	7ns	
T_{hd_LE}	7ns	
T_{sw_LE}	10ns	
T_{su_SDI}	3ns	
T_{hd_SDI},	3ns	

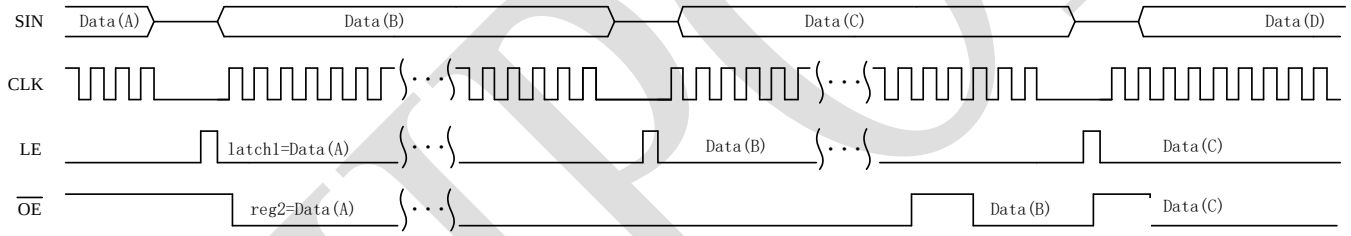
Dual Latch for higher refresh rate

Usual constant current LED sink driver timing diagrams



1. When display a high bit data, display time may far longer than data transfer time, next data transfer should wait display over.
2. When display a low bit data, display time may far shorter than data transfer time, next display should wait data transfer over.

ICND2037S dual latch timing diagrams



ICND2037S dual latch timing diagrams, data (A) and data (C) are high bit data, data (B) and data (D) are high bit data. Use the free time of display to transfer date could get higher refresh rate.

1. After data(A) transfer over, LE provide a latch signal,latch data(A)
2. After data(A) latched, $\overline{OE}$ from 1to 0， display data(A)
3. When display data(A),transfer data(B)
4. After data(B) transfer over, LE provide a latch signal， latch data(B),then transfer data(C)
5. After data(A) displayed, display data(B)
6. After data(A) transfer over, finish display data(B)
7. Latch data(C) and transfer data(D)

Maximum Ratings (T_a =25℃)

Characteristics	Symbol	Rating	Unit
Supply Voltage	V_{DD}	0~7	V
Output Current	I_O	25	mA
Input Voltage	V_{IN}	−0.4~V_{DD}+0.4	V
Output voltage	V_{OUT}	11V	
Clock Frequency	F_{CLK}	25	MHz
GND Terminal Current	I_{GND}	+5000	mA
Power Dissipation (On 4 Layer PCB，25℃)	P_D	1.98	W
Thermal Resistance	$R_{th(j-a)}$	64	℃/W
Junction Temperature	T_j	150	℃
Operating Temperature	T_{opr}	−40 ~ 85	℃
Storage Temperature	T_{stg}	−55 ~ 150	℃

DC Items (Unless otherwise specified, T_a =-40℃~85℃)

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	−	3.3	5	6.0	V
Output Voltage when ON	$V_{O(ON)}$	$\overline{OUTn}$	0.6	−	4	V
High level logic input voltage	V_{IH}	−	0.7*V_{DD}	−	V_{DD}	V
Low level logic input voltage	V_{IL}	−	GND	−	0.3*V_{DD}	V
SOUT high level output Current	I_{OH}	V_{DD}=5V	−	−	−1	mA
SOUT low level output Current	I_{OL}	V_{DD}=5V	−	−	1	mA
Constant current output	I_O	$\overline{OUTn}$	2	−	25	mA

Transition Items (Unless otherwise specified, V_{DD}=5V，T_a =-40℃~85℃)

Characteristics	Symbol	Test circuit	Test Conditions	Min	Typ	Max	Unit
Serial data transfer frequency	F_{CLK}	6	–	–	–	25	MHz
Clock pulse width	t_{wCLK}	6	SCK=H or L	20	–	–	ns
Latch pulse width	t_{wLE}	6	LE=H	20	–	–	ns
Enable pulse width	t_{wOE}	6	$\overline{OE}$ =H or L, R_{EXT}=890Ω	40	–	–	ns
Hold time	t_{HOLD1}	6	–	5	–	–	ns
	t_{HOLD2}	6	–	5	–	–	ns
Setup time	t_{SETUP1}	6	–	5	–	–	ns
	t_{SETUP2}	6	–	5	–	–	ns

Transition Items (Unless otherwise specified, V_{DD}=3.3V，T_a =-40℃~85℃)

Characteristics	Symbol	Test circuit	Test Conditions	Min	Typ	Max	Unit
Serial data transfer frequency	F_{CLK}	6	–	–	–	25	MHz
Clock pulse width	t_{wCLK}	6	SCK=H or L	25	–	–	ns
Latch pulse width	t_{wLE}	6	LE=H	25	–	–	ns
Enable pulse width	t_{wOE}	6	$\overline{OE}$ =H or L, R_{EXT}=890Ω	45	–	–	ns
Hold time	t_{HOLD1}	6	–	7	–	–	ns
	t_{HOLD2}	6	–	7	–	–	ns
Setup time	t_{SETUP1}	6	–	7	–	–	ns
	t_{SETUP2}	6	–	7	–	–	ns

Electrical Characteristics (Unless otherwise specified, V_{DD} =5V，T_a =25℃)

Characteristics	Symbol	Test circuit	Test Conditions	Min	Typ	Max	Unit
High level logic output voltage	V_{OH}	1	I_{OH}=-1mA, SOUT	V_{DD}-0.4	–	V_{DD}	V
Low level logic output voltage	V_{OL}	1	I_{OH}=+1mA, SOUT	–	–	0.4	V
High level logic input current	I_{IH}	2	V_{IN}=V_{DD}, $\overline{OE}$, SIN, CLK	–	–	1	μA
Low level logic input circuit	I_{IL}	3	V_{IN}=GND, LE, SIN, CLK	–	–	-1	μA
Power supply current	I_{DD1}	4	Rext=Open, OUT off	–	1.7	–	mA
	I_{DD2}	4	Rext=1.24KΩ, OUT off	–	0.13	–	mA
	I_{DD3}	4	Rext=10KΩ, OUT off	–	0.13	–	mA
	I_{DD4}	4	Rext=1.24KΩ, OUT on	–	5.5	–	mA
	I_{DD5}	4	Rext=10KΩ, OUT on	–	3.3	–	mA
Constant current output	I_{O1}	5	V_{DD}=5.0V, V_O=1.0V, R_{EXT}=1.23kΩ	–	15	–	mA

Constant current error	ΔI_O	5	V_{DD}=5.0V, V_O=1.0V, R_{EXT}=1.23kΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$	–	±0.37	±0.52	mA
Constant current power supply voltage regulation	$\%V_{DD}$	5	V_{DD}=4.5~5.5V, V_O=1.0V, R_{EXT}=1.24kΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$	–	±0.2	–	%/V
Constant current output voltage regulation	$\%V_{OUT}$	5	V_{DD}=5.0V, V_O=1.0~3.0V, R_{EXT}=1.24kΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$	–	±0.1		%/V
Pull-up resistor	R_{UP}	3	$\overline{OE}$	250	500	800	kΩ
Pull-down resistor	R_{DOWN}	2	LE	250	500	800	kΩ

Electrical Characteristics (Unless otherwise specified, V_{DD} =3.3V，T_a =25℃)

Characteristics	Symbol	Test circuit	Test Conditions	Min	Typ	Max	Unit
High level logic output voltage	V_{OH}	1	I_{OH}=-1mA, SOUT	V_{DD}-0.4	–	V_{DD}	V
Low level logic output voltage	V_{OL}	1	I_{OH}=+1mA, SOUT	–	–	0.4	V
High level logic input current	I_{IH}	2	V_{IN}=V_{DD}, $\overline{OE}$, SIN, CLK	–	–	1	μA
Low level logic input circuit	I_{IL}	3	V_{IN}=GND, LE, SIN, CLK	–	–	-1	μA
Power supply current	I_{DD1}	4	Rext=Open, OUT off	–	1.9	–	mA
	I_{DD2}	4	Rext=1.24KΩ, OUT off	–	0.13	–	mA
	I_{DD3}	4	Rext=10KΩ, OUT off	–	0.13	–	mA
	I_{DD4}	4	Rext=1.24KΩ, OUT on	–	5.6	–	mA
	I_{DD5}	4	Rext=10KΩ, OUT on	–	3.4	–	mA
Constant current output	I_{O1}	5	V_{DD}=5.0V, V_O=1.0V, R_{EXT}=1.23kΩ	–	15	–	mA
Constant current error	ΔI_O	5	V_{DD}=5.0V, V_O=1.0V, R_{EXT}=1.23kΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$	–	±0.37	±0.52	mA
Constant current power supply voltage regulation	$\%V_{DD}$	5	V_{DD}=4.5~5.5V, V_O=1.0V, R_{EXT}=1.24kΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$	–	±0.2	–	%/V
Constant current output voltage regulation	$\%V_{OUT}$	5	V_{DD}=5.0V, V_O=1.0~3.0V, R_{EXT}=1.24kΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$	–	±0.1		%/V
Pull-up resistor	R_{UP}	3	$\overline{OE}$	250	500	800	kΩ
Pull-down resistor	R_{DOWN}	2	LE	250	500	800	kΩ

Switching Characteristics (Unless otherwise specified, T_a =25℃, V_{DD} =5.0V)

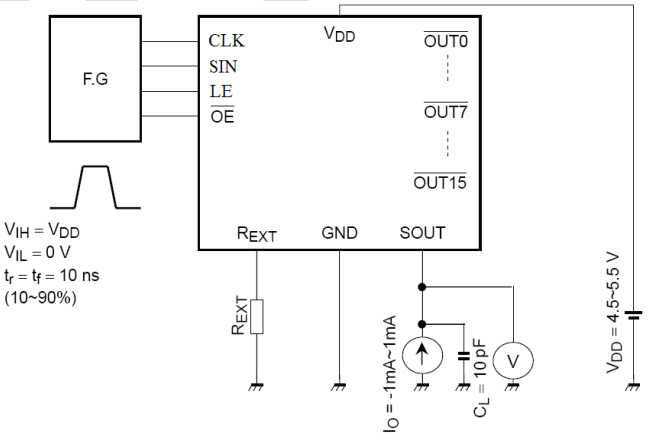
Characteristics		Symbol	Test circuit	Test conditions	Min	Typ	Max	Unit
Propagation delay time	$\overline{OE}$ – $\overline{OUT0}$	t_{pLH3}	6	LE=H	–	33	–	ns
	$\overline{OE}$ – $\overline{OUT1}$	t_{pHL3}	6	LE=H	–	35	–	
	CLK–SOUT	t_{pHL}	6	-	–	28	–	
Output rise time		t_{or}	6	10~90% of voltage waveform	–	18	–	ns
Output fall time		t_{of}	6	90~10% voltage waveform	–	15	–	ns

Switching Characteristics (Unless otherwise specified, T_a =25℃, V_{DD} =3.3V)

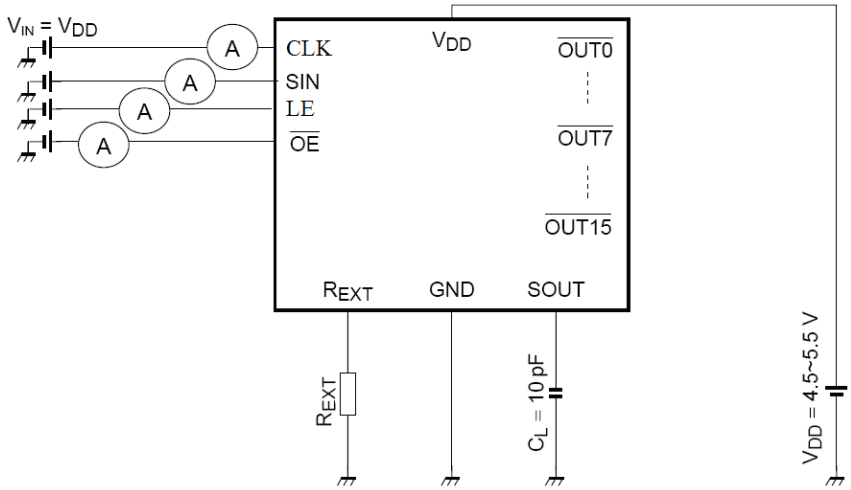
Characteristics		Symbol	Test circuit	Test conditions	Min	Typ	Max	Unit
Propagation delay time	$\overline{OE}$ – $\overline{OUT0}$	t_{pLH3}	6	LE=H	–	35	–	ns
	$\overline{OE}$ – $\overline{OUT1}$	t_{pHL3}	6	LE=H	–	38	–	
	CLK–SOUT	t_{pHL}	6	-	–	31	–	
Output rise time		t_{or}	6	10~90% of voltage waveform	–	20	–	ns
Output fall time		t_{of}	6	90~10% voltage waveform	–	18	–	ns

Test Circuit

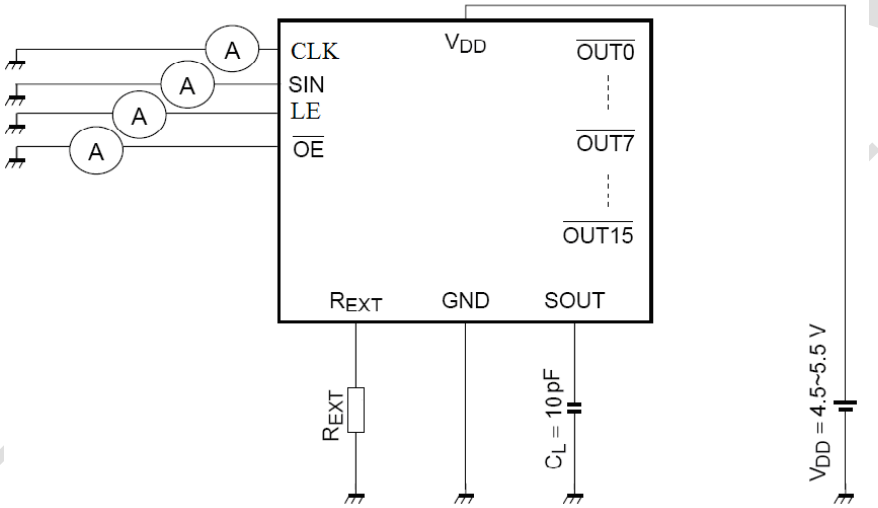
Test Circuit1: High level logic input voltage/Low level logic input voltage



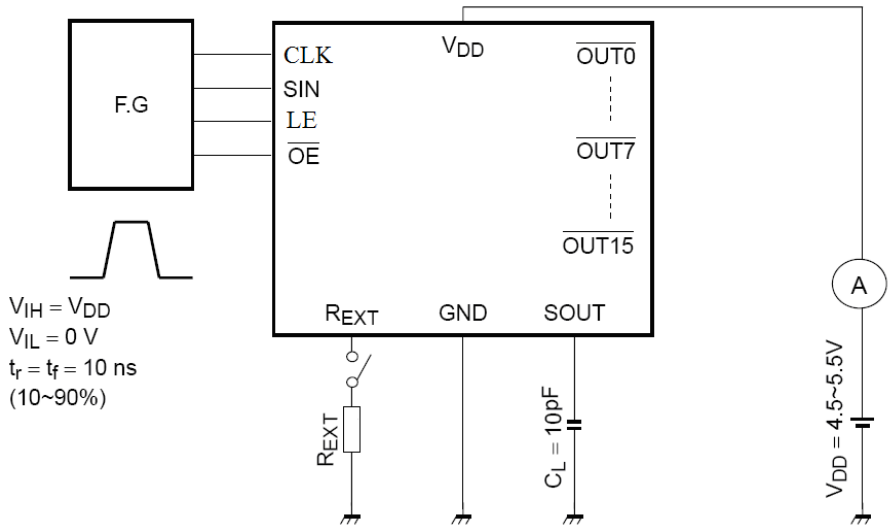
Test Circuit2: High level logic input current/Pull-down resistor



Test Circuit3：Low level logic input current/Pull-up resistor

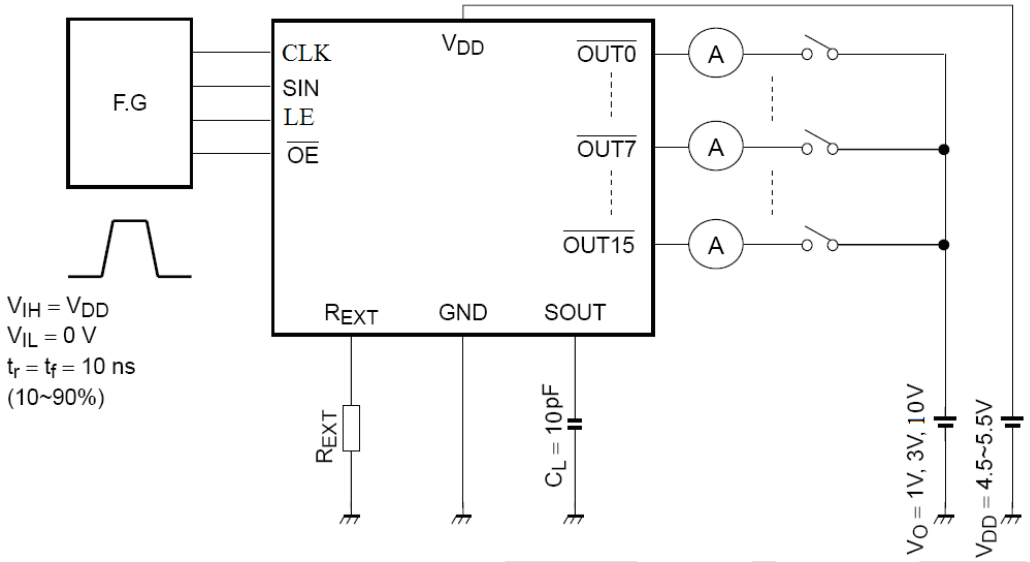


Test Circuit4: Power supply current

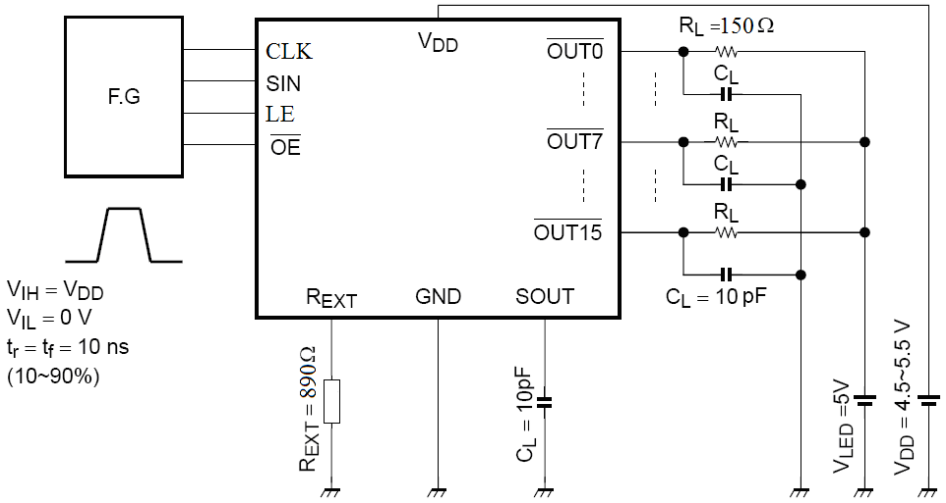


Test Circuit5: Constant current output/Output OFF leak current/Constant current error

Constant current power supply voltage regulation/Constant current output voltage regulation

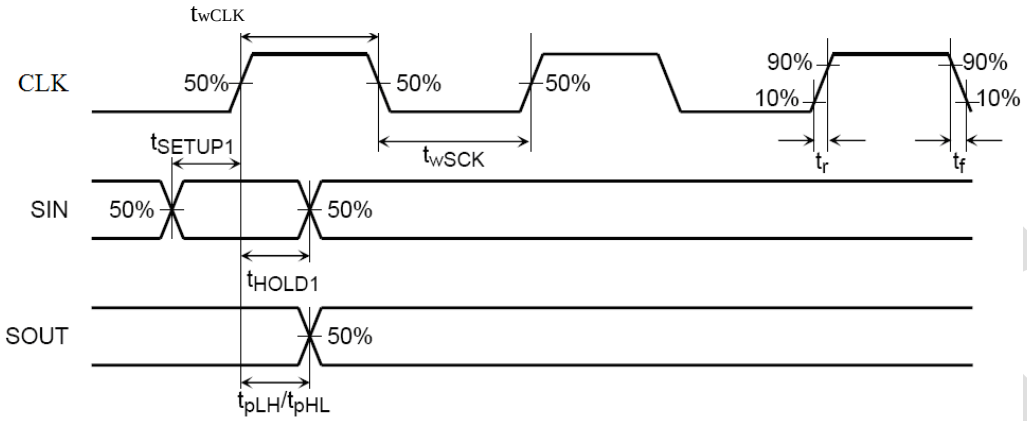


Test Circuit6: Switching Characteristics

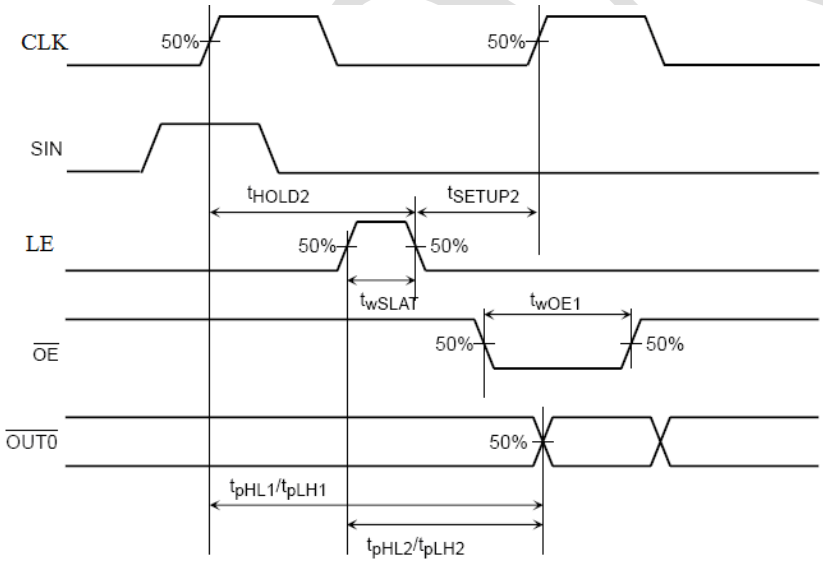


Timing Waveforms

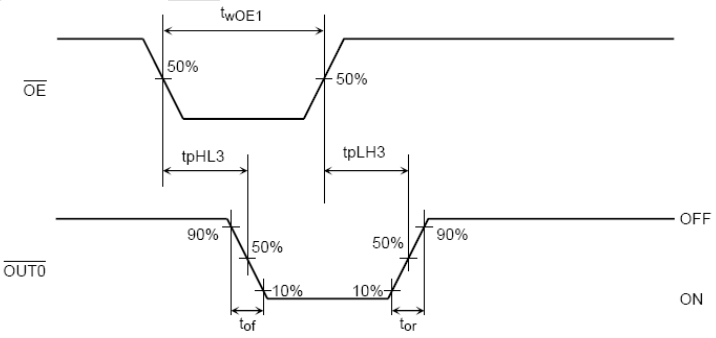
1. CLK, SIN, SOUT



2. CLK, SIN, LE, $\overline{OE}$, $\overline{OUT0}$



3. $\overline{OUT0}$

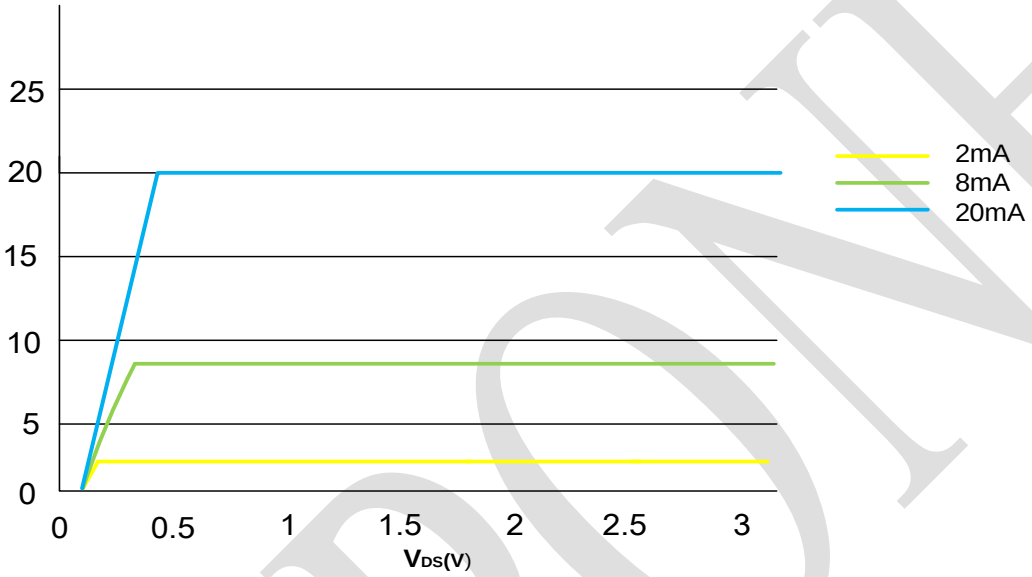


Application Information

ICND2037S exploits current precision controlling technology，and provides nearly no current variations from channel to channel and from IC to IC.

1) The maximum current variation between channels is less than ±3.0%，and that between ICs<±3.5%.

2) The current characteristic of output stage is flat, and can be kept constant regardless of the variations of LED forward voltage.



Setting Output Current

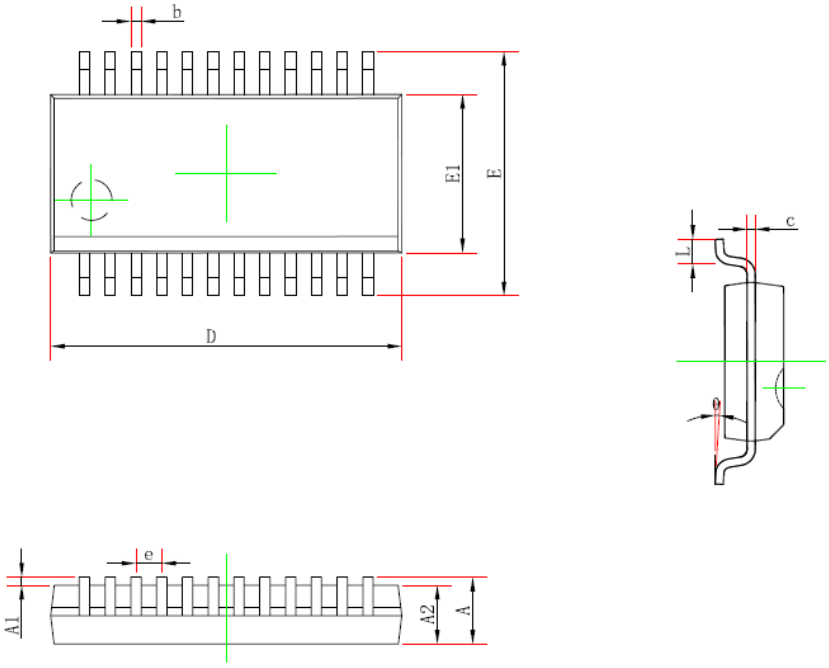
The output current (I_{out}) of ICND2037S is set by an external resistor, R_{ext}. The relationship between I_{out} and R_{ext} is

$$I_{out}=(V_{R\text{-}EXT}/ R_{ext})*15 \quad （Gain=100%） \quad V_{R\text{-}EXT}=1.24V；$$

Package Outline

SSOP24-P-150-0.64

SSOP24 (150mil) PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
A	——	1.750	——	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	——	0.049	——
b	0.203	0.305	0.008	0.012
c	0.102	0.254	0.004	0.010
D	8.450	8.850	0.333	0.348
E1	3.800	4.000	0.150	0.157
E	5.800	6.200	0.228	0.244
e	0.635(BSC)		0.025(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Product Ordering Information

Product number	Package （Pb-Free）	Weight（mg）
ICND2037S	SSOP24-P-150-0.635	130

Revision History

Rev	Date	Description
1.0	2020/05	Initial Release

Important information

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