CHIPONE

集创北方

ICND2038S

(16-Channel Constant Current LED Sink Driver with Dual Latch)

Description

The ICND2038S is a 16-channel constant current sink output LED driver. All 16-channels constant current can be set by a single external resistor, which provides users flexibility in controlling the light intensity of LEDs.

The ICND2038S exploits current precision controlling technology , which makes error between ICs less than ±2.0%, and error between channels less than ±2.0%. At ICND2038S output stage , 16-regulated output ports are designed to provide uniform and constant current sinks for driving LEDs within a large range of forward voltage(VF) variations.

ICND2038S contains two 16-bit shift registers and latches which convert serial input data into parallel output format. For integrated dual latches, ICND2038S could get higher refresh rate.

Features

- ✧ 16-channel constant current output
- ✧ Output current setting range：
  0.5~45mA×16@V_{DD}=5V constant current output
  0.5~25mA×16@V_{DD}=3.3Vconstant current output
- ✧ Current accuracy
  Between channel :< ±2.0%
  Between ICs :< ± 2.0%
- ✧ Fast response of output current,
  $\overline{OE}$ (min):40ns@V_{DD}=5V
- ✧ I/O: Schmitt trigger input
- ✧ Data transfer frequency:f_{MAX}=30MHz(Max)
- ✧ Power supply voltage: VDD=3.3～5V
- ✧ Operating Temperature: –40°C to +85°C
- ✧ 4 bit current gain：25%~100%
- ✧ Adjustable Pre-Charge for Ghosting Reduction
- ✧ LED Protection Circuit
- ✧ Low-Gray Scale Enhancement
- ✧ Integrated Dual Latches for higher refresh rate
- ✧ Dim line at the first scan line

Package

Shrink SOP

SSOP24-150-0.635

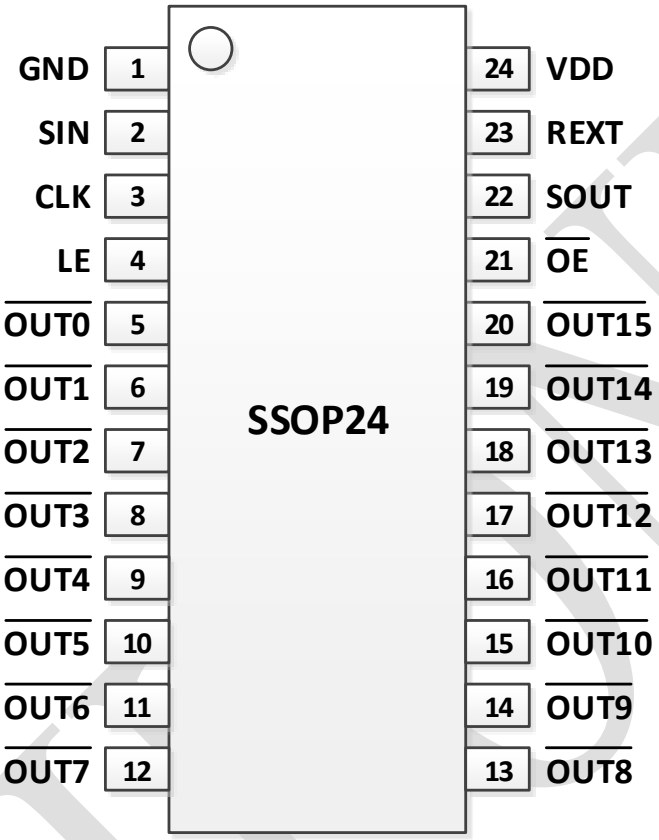
Quad Flat No-Lead

QFN24-4*4-0.5

ICND2038S

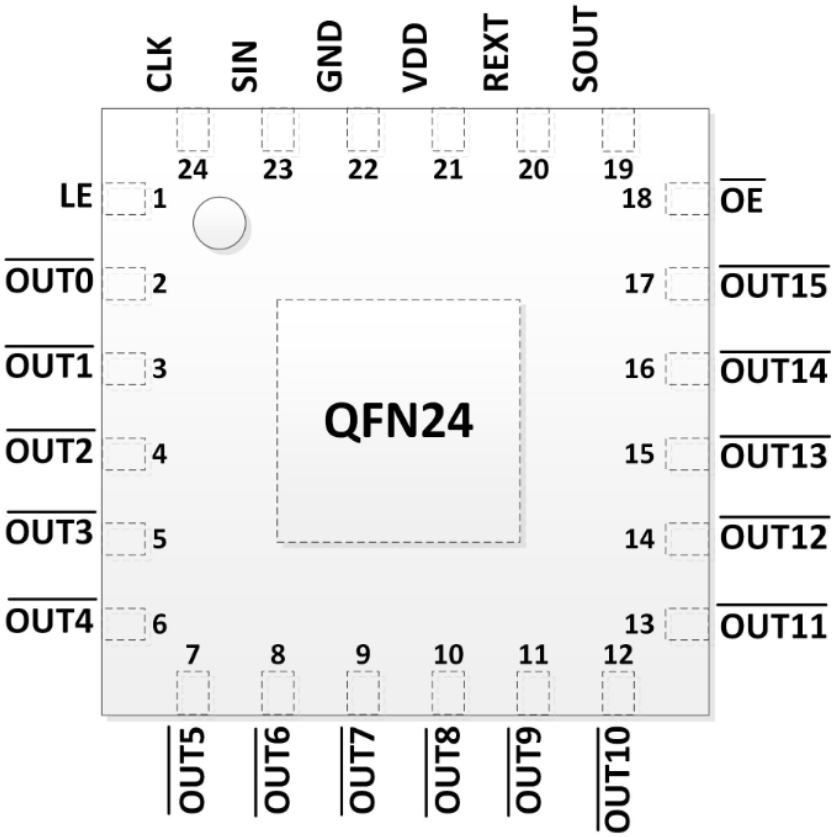
Pin Configuration

1 SSOP24-P-150-0.635



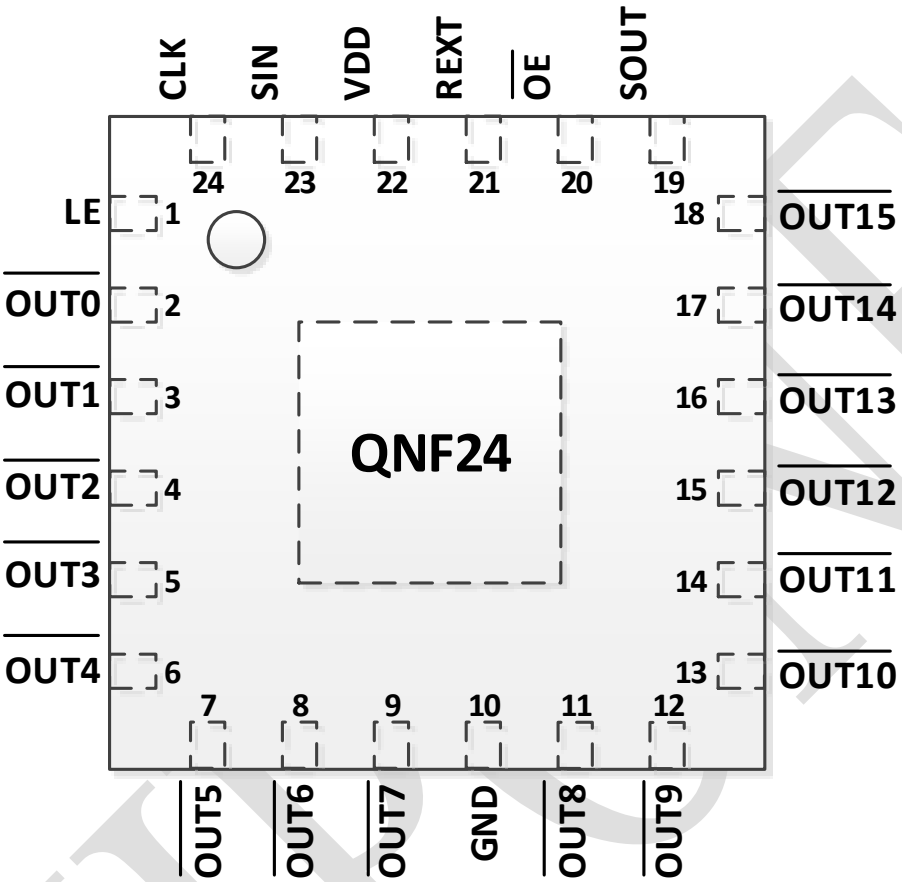
ICND2038S (SSOP24)		
Pin No.	Pin Name	Function
1	GND	Power Ground
2	SIN	Serial data or command input for driver control
3	CLK	Clock input terminal for data shift on rising edge
4	LE	The command parser is a counter of LE length: A different length of LE indicates a different command.
5～20	$\overline{OUT0}$ ~ $\overline{OUT15}$	Constant current output
21	$\overline{OE}$	Output enable terminal, $\overline{OE}$ low level, all output drivers are turned ON ; $\overline{OE}$ high level, all output drivers are turned OFF
22	SOUT	Serial-data or command output to the following IC.
23	R-EXT	Constant-current value setting .Connection to an external resistor to GND.
24	VDD	Power-supply voltage

2 QFN24-4*4-0.5



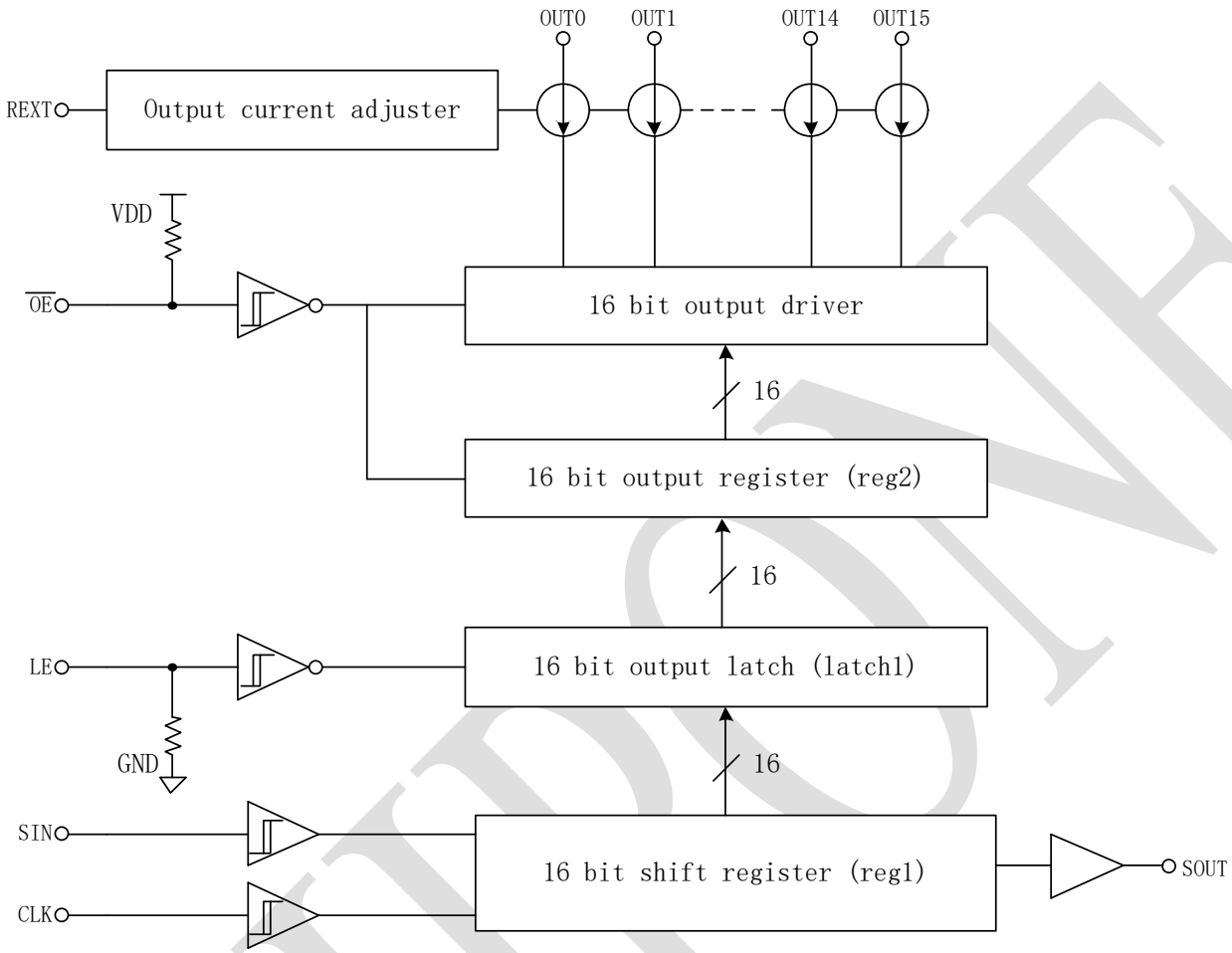
ICND2038SGN-01 (QFN24)		
Pin No.	Pin Name	Function
1	LE	The command parser is a counter of LE length: A different length of LE indicates a different command
2～17	$\overline{OUT0}$ ~ $\overline{OUT15}$	Constant current output
18	$\overline{OE}$	Output enable terminal, $\overline{OE}$ low level, all output drivers are turned ON ; $\overline{OE}$ high level, all output drivers are turned OFF
19	SOUT	Serial-data or command output to the following IC
20	R-EXT	Constant-current value setting .Connection to an external resistor to GND
21	VDD	Power-supply voltage
22	GND	Power Ground
23	SIN	Serial data or command input for driver control
24	CLK	Clock input terminal for data shift on rising edge

3 QFN24-4*4-0.5



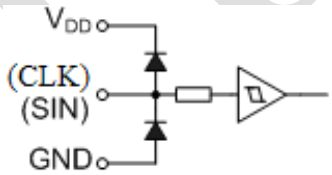
ICND2038SGN-02 (QFN24)		
Pin No.	Pin Name	Function
1	LE	The command parser is a counter of LE length: A different length of LE indicates a different command
2～9，11~18	$\overline{OUT0}$ ~ $\overline{OUT15}$	Constant current output
10	GND	Power Ground
19	SOUT	Serial-data or command output to the following IC
20	$\overline{OE}$	Output enable terminal, $\overline{OE}$ low level, all output drivers are turned ON ; $\overline{OE}$ high level, all output drivers are turned OFF
21	R-EXT	Constant-current value setting .Connection to an external resistor to GND
22	VDD	Power-supply voltage
23	SIN	Serial data or command input for driver control
24	CLK	Clock input terminal for data shift on rising edge

Block Diagram

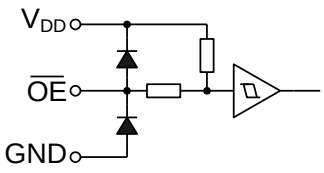


I/O Equivalent Circuits

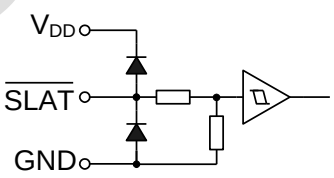
1. CLK, SIN



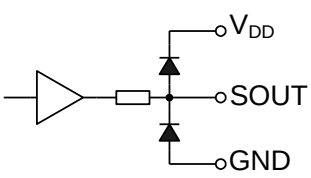
2. $\overline{OE}$



3. LE



4. SOUT



Shift-Register and Command Parser

A simple 16bit shift-register is integrated. All data, such as gray scale and configuration, are latched by the shift-register.

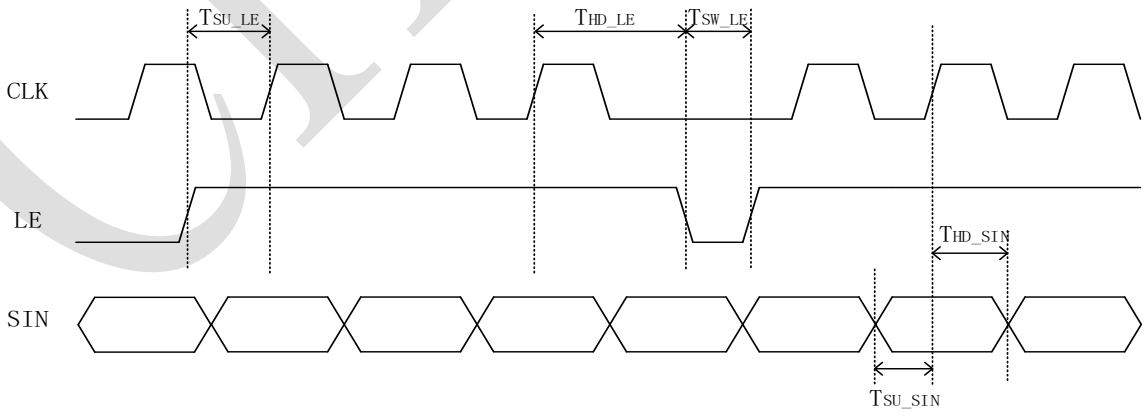
The command parser is a counter of LE length: A different length of LE indicates a different command. Such as a 3bit LE is a “Data Latch” command which indicates that there is a gray scale written in. It will send the 16bit data on shift-register to SRAM.

Control Command

Command Name	Number of DCLK Rising Edge when LE is High	Description
RESET	0	Reg Reset to default setting
DATA_LATCH	1&2	Transfer Serial data to buffers（reg2_bit[6]=1
	3	Transfer Serial data to buffers（reg2_bit[6]=0）
--	4~10	Reserved
WR_REG1	11	Write Configuration Register 1
WR_REG2	12	Write Configuration Register 2

Note1：The length of LE is defined as this: How many positive-edges of DCLK when LE stays logic “1”. For example, the first pulse of LE in the next figure is show a length of 3, which is a “Data Latch” command.

LE waveforms

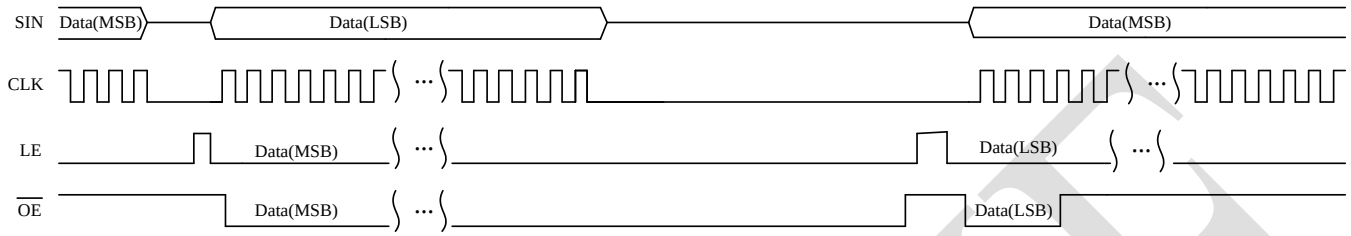


Hold time

Name	MIN	Note
T_{su_LE}	7ns	
T_{hd_LE}	7ns	
T_{sw_LE}	10ns	
T_{su_SDI}	3ns	
T_{hd_SDI},	3ns	

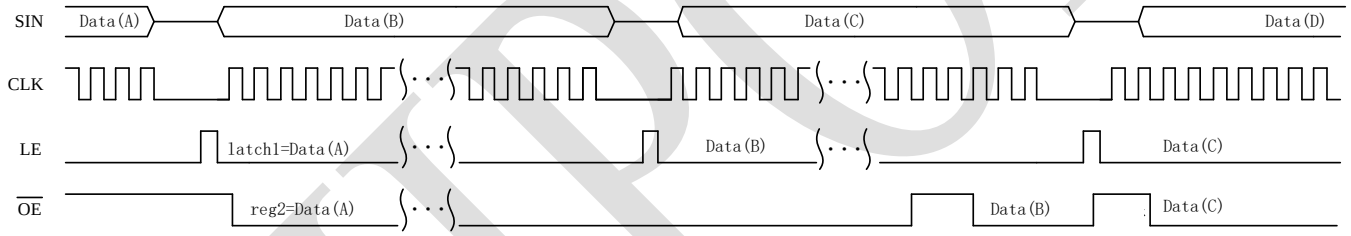
Dual Latch for higher refresh rate

Usual constant current LED sink driver timing diagrams



1. When display a high bit data, display time may far longer than data transfer time, next data transfer should wait display over.
2. When display a low bit data, display time may far shorter than data transfer time, next display should wait data transfer over.

ICND2038S dual latch timing diagrams



ICND2038S dual latch timing diagrams, data (A) and data (C) are high bit data, data (B) and data (D) are high bit data. Use the free time of display to transfer date could get higher refresh rate.

1. After data(A) transfer over, LE provide a latch signal,latch data(A)
2. After data(A) latched, $\overline{OE}$ from 1to 0， display data(A)
3. When display data(A),transfer data(B)
4. After data(B) transfer over, LE provide a latch signal， latch data(B),then transfer data(C)
5. After data(A) displayed, display data(B)
6. After data(A) transfer over, finish display data(B)
7. Latch data(C) and transfer data(D)

Maximum Ratings (T_a =25℃)

Characteristics		Symbol	Rating	Unit
Supply Voltage		V_{DD}	0~7	V
Output Current		I_O	45	mA
Input Voltage		V_{IN}	−0.4~V_{DD}+0.4	V
Output voltage		V_{OUT}	11V	
Clock Frequency		F_{CLK}	30	MHz
GND Terminal Current		I_{GND}	+1000	mA
Power Dissipation (On PCB，25℃)	DN-type	P_D	3.19	W
Thermal Resistance	DN-type	$R_{th(j-a)}$	39.15	℃/W
Operating Temperature		T_{opr}	−40 ~ 85	℃
Storage Temperature		T_{stg}	−55 ~ 150	℃

DC Items (Unless otherwise specified, T_a =-40℃~85℃)

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	−	3.3	5	6.0	V
Output Voltage when ON	$V_{O(ON)}$	$\overline{OUTn}$	0.6	−	4	V
High level logic input voltage	V_{IH}	−	0.7*V_{DD}	−	V_{DD}	V
Low level logic input voltage	V_{IL}	−	GND	−	0.3*V_{DD}	V
SOUT high level output Current	I_{OH}	V_{DD}=5V	−	−	−1	mA
SOUT low level output Current	I_{OL}	V_{DD}=5V	−	−	1	mA
Constant current output	I_O	$\overline{OUTn}$	0.5	−	45	mA

Transition Items (Unless otherwise specified, V_{DD}=5V，T_a =-40℃~85℃)

Characteristics	Symbol	Test circuit	Test Conditions	Min	Typ	Max	Unit
Serial data transfer frequency	F_{CLK}	6	–	–	–	30	MHz
Clock pulse width	t_{wCLK}	6	SCK=H or L	20	–	–	ns
Latch pulse width	t_{wLE}	6	LE=H	20	–	–	ns
Enable pulse width	t_{wOE}	6	$\overline{OE}$ =H or L, R_{EXT}=890Ω	40	–	–	ns
Hold time	t_{HOLD1}	6	–	5	–	–	ns
	t_{HOLD2}	6	–	5	–	–	ns
Setup time	t_{SETUP1}	6	–	5	–	–	ns
	t_{SETUP2}	6	–	5	–	–	ns
Maximum clock rise time	t_r	6		–	–	500	ns
Maximum clock fall time	t_f	6		–	–	500	ns

Transition Items (Unless otherwise specified, V_{DD}=3.3V，T_a =-40℃~85℃)

Characteristics	Symbol	Test circuit	Test Conditions	Min	Typ	Max	Unit
Serial data transfer frequency	F_{CLK}	6	–	–	–	25	MHz
Clock pulse width	t_{wCLK}	6	SCK=H or L	25	–	–	ns
Latch pulse width	t_{wLE}	6	LE=H	25	–	–	ns
Enable pulse width	t_{wOE}	6	$\overline{OE}$ =H or L, R_{EXT}=890Ω	45	–	–	ns
Hold time	t_{HOLD1}	6	–	7	–	–	ns
	t_{HOLD2}	6	–	7	–	–	ns
Setup time	t_{SETUP1}	6	–	7	–	–	ns
	t_{SETUP2}	6	–	7	–	–	ns
Maximum clock rise time	t_r	6		–	–	500	ns
Maximum clock fall time	t_f	6		–	–	500	ns

Electrical Characteristics (Unless otherwise specified, V_{DD} =5V，T_a =25℃)

Characteristics	Symbol	Test circuit	Test Conditions	Min	Typ	Max	Unit
High level logic output voltage	V_{OH}	1	I_{OH}=-1mA, SOUT	V_{DD}-0.4	–	V_{DD}	V
Low level logic output voltage	V_{OL}	1	I_{OH}=+1mA, SOUT	–	–	0.4	V
High level logic input current	I_{IH}	2	V_{IN}=V_{DD}, $\overline{OE}$, SIN, CLK	–	–	1	μA
Low level logic input circuit	I_{IL}	3	V_{IN}=GND, LE, SIN, CLK	–	–	-1	μA
Power supply current	I_{DD1}	4	Rext=Open, OUT off	–	2.7	5.8	mA
	I_{DD2}	4	Rext=1.24KΩ, OUT off	–	4.8	7.3	mA
	I_{DD3}	4	Rext=620Ω, OUT off	–	6.3	9.2	mA

	I_{DD4}	4	Rext=1.24KΩ, OUT on	–	5.5	8.7	mA
	I_{DD5}	4	Rext=620Ω, OUT on	–	6.6	9.7	mA
Constant current output	I_{O1}	5	V_{DD}=5.0V, V_O=1.0V, R_{EXT}=1.23kΩ	–	15	–	mA
	I_{O2}	5	V_{DD}=5.0V, V_O=1.0V, R_{EXT}=615Ω	–	30	–	mA
Constant current error	ΔI_O	5	V_{DD}=5.0V, V_O=1.0V, R_{EXT}=1.23kΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$	–	± 0.15	±0.37	mA
Constant current power supply voltage regulation	$\%V_{DD}$	5	V_{DD}=4.5~5.5V, V_O=1.0V, R_{EXT}=1.24kΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$	–	± 0.2	–	%/V
Constant current output voltage regulation	$\%V_{OUT}$	5	V_{DD}=5.0V, V_O=1.0~3.0V, R_{EXT}=1.24kΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$	–	± 0.1		%/V
Pull-up resistor	R_{UP}	3	$\overline{OE}$	250	500	800	kΩ
Pull-down resistor	R_{DOWN}	2	LE	250	500	800	kΩ

Electrical Characteristics (Unless otherwise specified, V_{DD} =3.3V, T_a =25℃)

Characteristics	Symbol	Test circuit	Test Conditions	Min	Typ	Max	Unit
High level logic output voltage	V_{OH}	1	I_{OH}=-1mA, SOUT	V_{DD}-0.4	–	V_{DD}	V
Low level logic output voltage	V_{OL}	1	I_{OH}=+1mA, SOUT	–	–	0.4	V
High level logic input current	I_{IH}	2	V_{IN}=V_{DD}, $\overline{OE}$, SIN, CLK	–	–	1	μA
Low level logic input circuit	I_{IL}	3	V_{IN}=GND, LE, SIN, CLK	–	–	-1	μA
Power supply current	I_{DD1}	4	Rext=Open, OUT off	–	2.3	–	mA
	I_{DD2}	4	Rext=1.24KΩ, OUT off	–	4.4	–	mA
	I_{DD3}	4	Rext=620Ω, OUT off	–	5.9	–	mA
	I_{DD4}	4	Rext=1.24KΩ, OUT on	–	5.1	–	mA
	I_{DD5}	4	Rext=620Ω, OUT on	–	6.2	–	mA
Constant current output	I_{O1}	5	V_{DD}=5.0V, V_O=1.0V, R_{EXT}=1.23kΩ	–	15	–	mA
	I_{O2}	5	V_{DD}=5.0V, V_O=1.0V, R_{EXT}=615Ω	–	25	–	mA
Constant current error	ΔI_O	5	V_{DD}=5.0V, V_O=1.0V, R_{EXT}=1.23kΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$	–	±0.15	±0.37	mA
Constant current power supply voltage regulation	$\%V_{DD}$	5	V_{DD}=4.5~5.5V, V_O=1.0V, R_{EXT}=1.24kΩ, $\overline{OUT0}$ ~ $\overline{OUT15}$	–	±0.2	–	%/V
Constant current output voltage regulation	$\%V_{OUT}$	5	V_{DD}=5.0V, V_O=1.0~3.0V, R_{EXT}=1.24kΩ,	–	±0.1		%/V

			$\overline{OUT0}$ ~ $\overline{OUT15}$				
Pull-up resistor	R_{UP}	3	$\overline{OE}$	250	500	800	kΩ
Pull-down resistor	R_{DOWN}	2	LE	250	500	800	kΩ

Switching Characteristics (Unless otherwise specified, T_a =25℃, V_{DD} =5.0V)

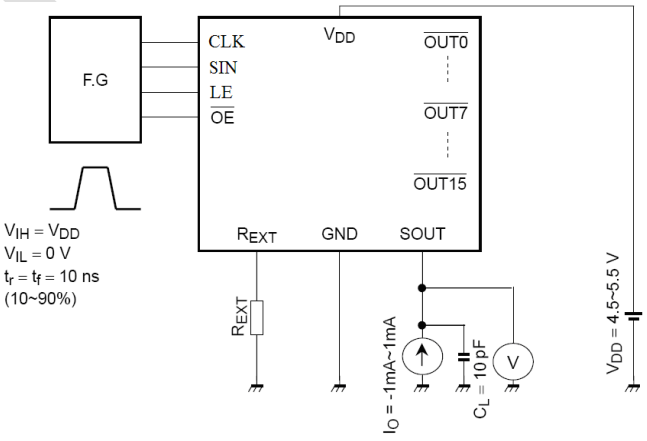
Characteristics		Symbol	Test circuit	Test conditions	Min	Typ	Max	Unit
Propagation delay time	$\overline{OE}$ - $\overline{OUT0}$	t_{pLH3}	6	LE=H	-	22	26	ns
	$\overline{OE}$ - $\overline{OUT1}$	t_{pHL3}	6	LE=H	-	22	25	
	CLK-SOUT	t_{pHL}	6	-	-	26	30	
Output rise time		t_{or}	6	10~90% of voltage waveform	-	25	28	ns
Output fall time		t_{of}	6	90~10% voltage waveform	-	33	37	ns

Switching Characteristics (Unless otherwise specified, T_a =25℃, V_{DD} =3.3V)

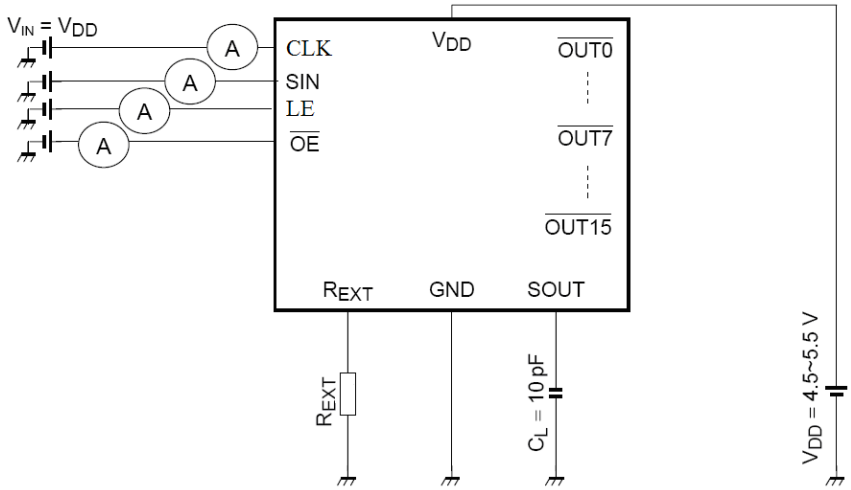
Characteristics		Symbol	Test circuit	Test conditions	Min	Typ	Max	Unit
Propagation delay time	$\overline{OE}$ - $\overline{OUT0}$	t_{pLH3}	6	LE=H	-	25	-	ns
	$\overline{OE}$ - $\overline{OUT1}$	t_{pHL3}	6	LE=H	-	26	-	
	CLK-SOUT	t_{pHL}	6	-	-	27	-	
Output rise time		t_{or}	6	10~90% of voltage waveform	-	28	-	ns
Output fall time		t_{of}	6	90~10% voltage waveform	-	36	-	ns

Test Circuit

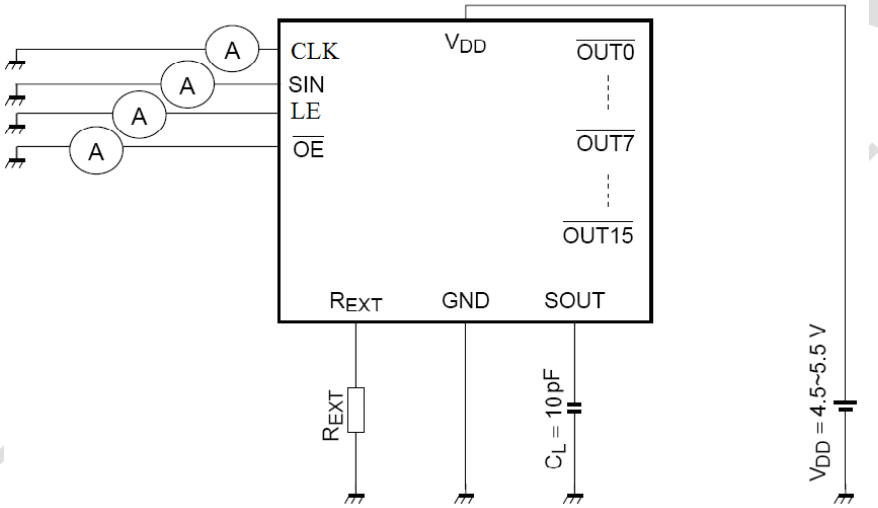
Test Circuit1: High level logic input voltage/Low level logic input voltage



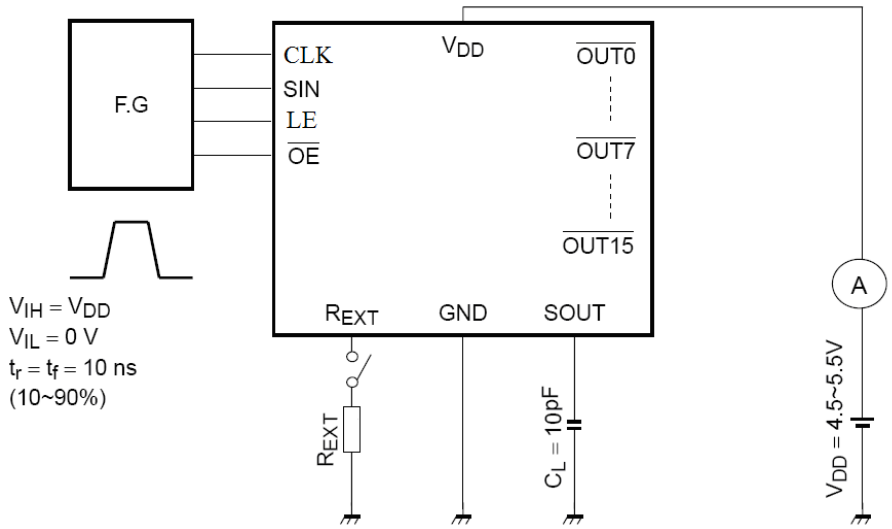
Test Circuit2: High level logic input current/Pull-down resistor



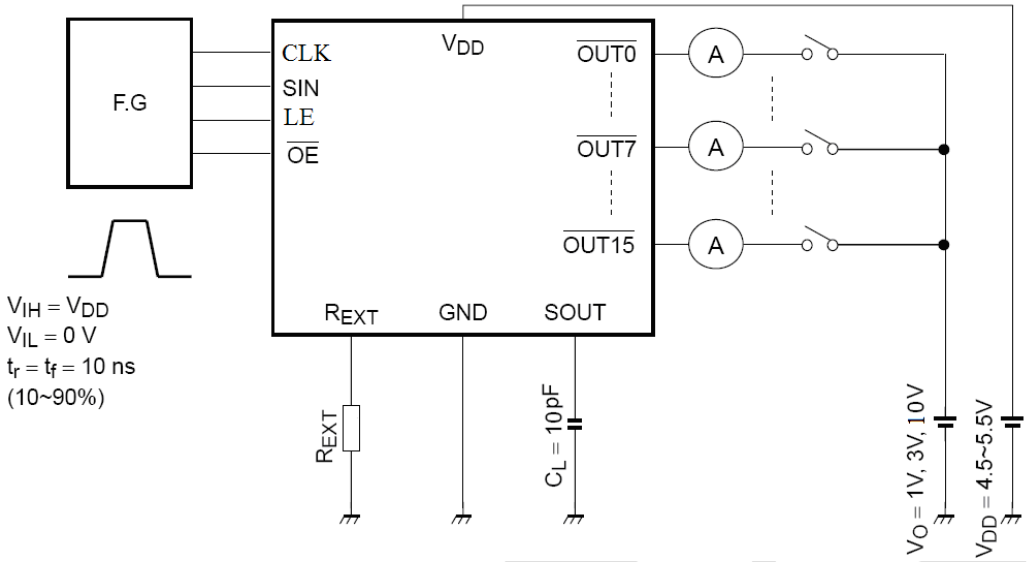
Test Circuit3：Low level logic input current/Pull-up resistor



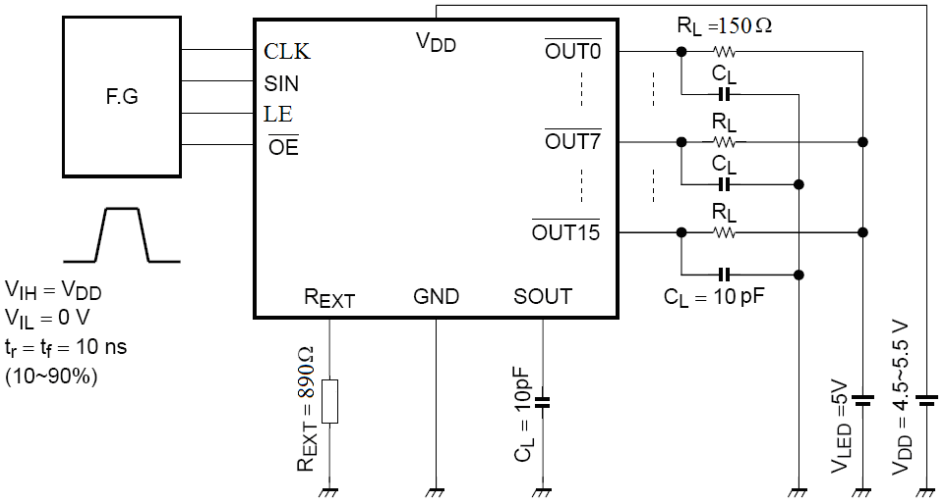
Test Circuit4: Power supply current



Test Circuit5: Constant current output/Output OFF leak current/Constant current error
Constant current power supply voltage regulation/Constant current output voltage regulation

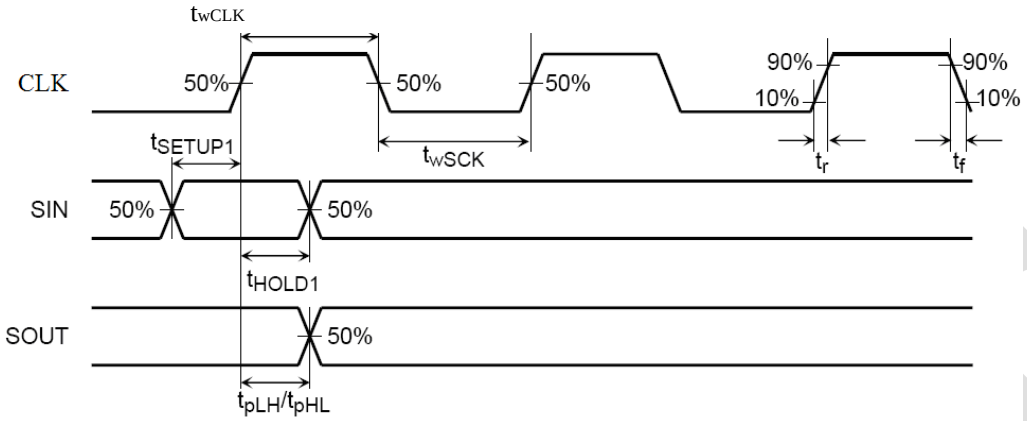


Test Circuit6: Switching Characteristics

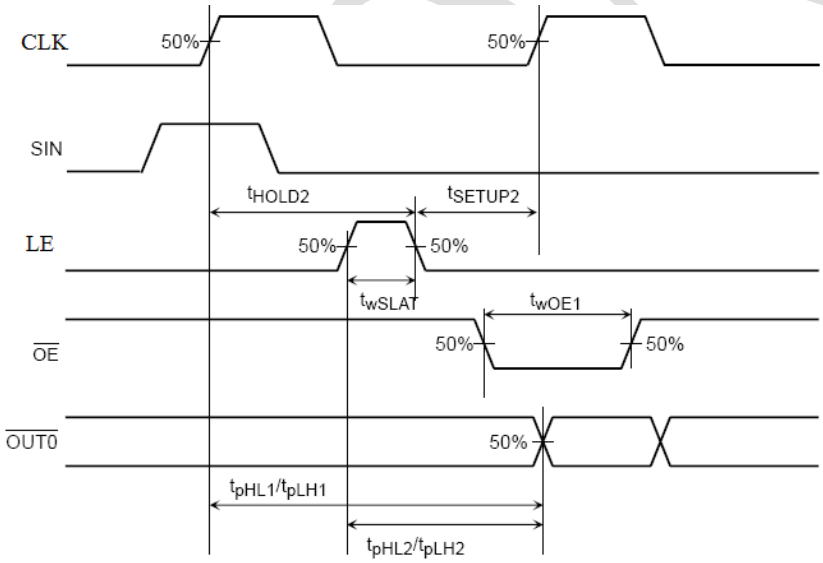


Timing Waveforms

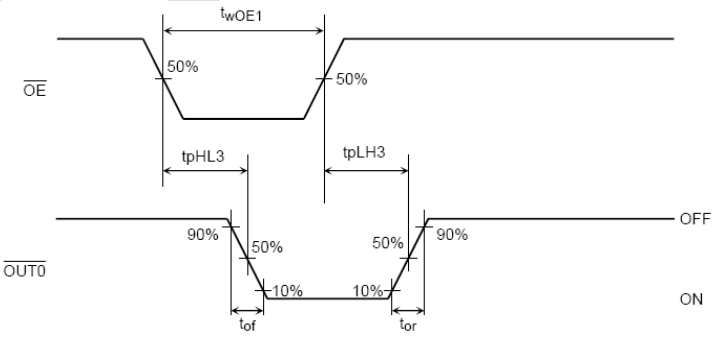
1. CLK, SIN, SOUT



2. CLK, SIN, LE, $\overline{OE}$, $\overline{OUT0}$



3. $\overline{OUT0}$



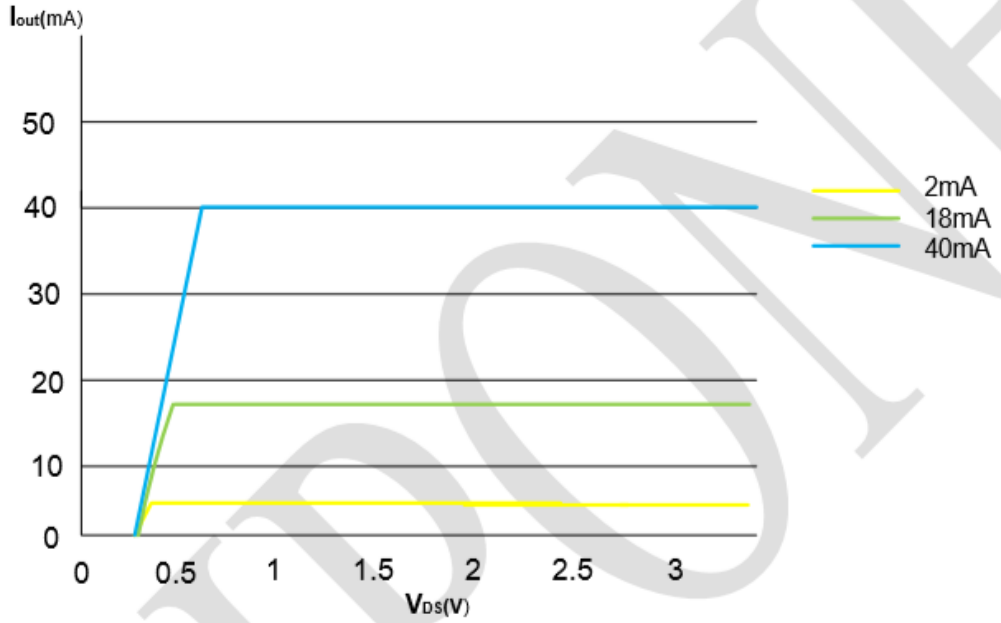
Application Information

ICND2038S exploits current precision controlling technology，and provides nearly no current variations from channel to channel and from IC to IC.

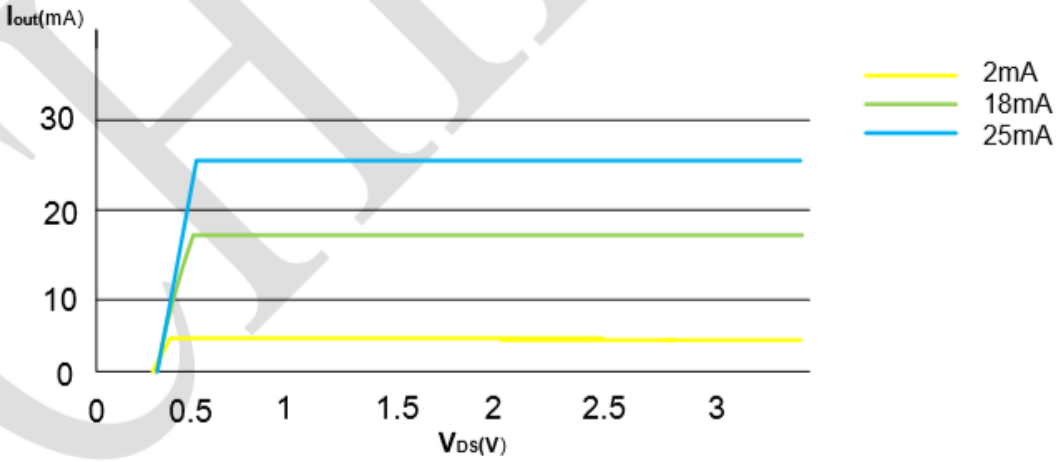
1) The maximum current variation between channels is less than ±2.0%，and that between ICs<±2.0%.

2) The current characteristic of output stage is flat, and can be kept constant regardless of the variations of LED forward voltage.

VDD=5V



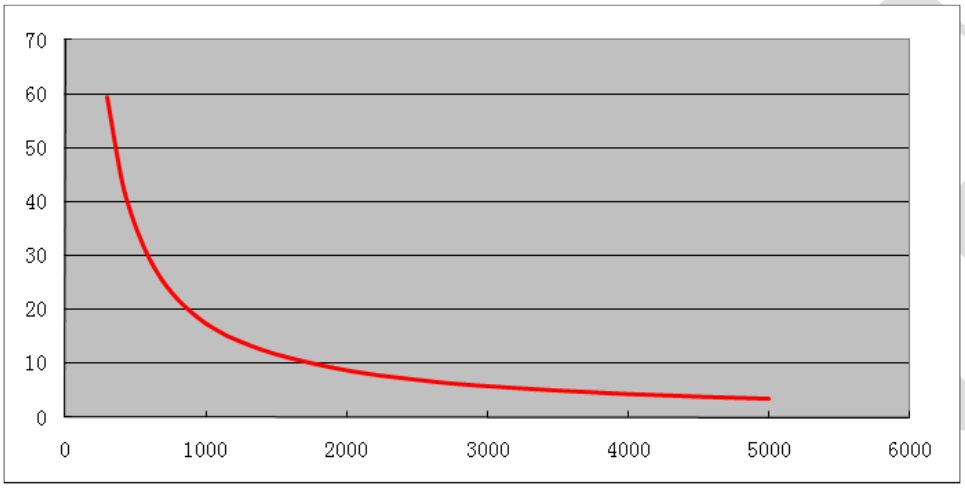
VDD=3.3V



Setting Output Current

The output current (I_{out}) of ICND2038S is set by an external resistor, R_{ext}. The relationship between I_{out} and R_{ext} is

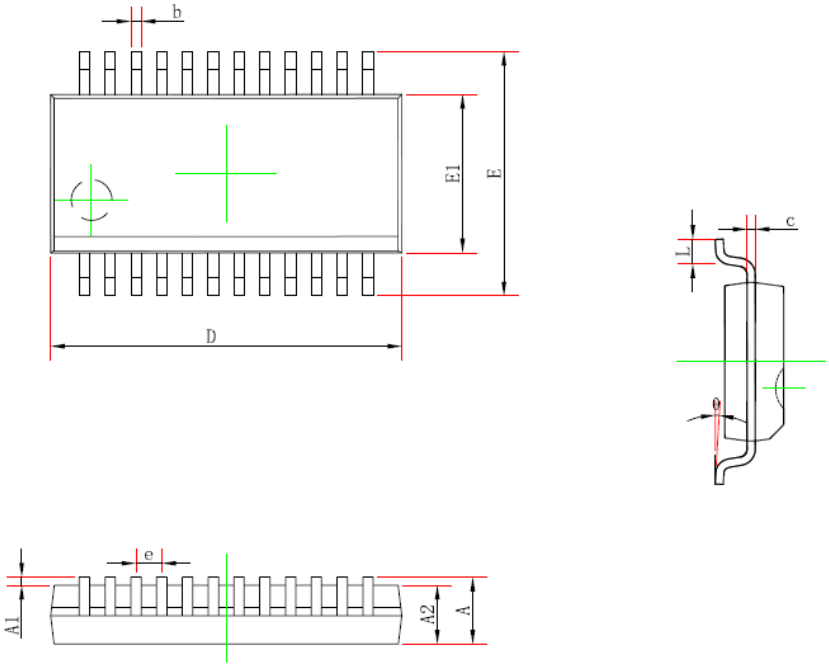
$$Iout=(V_{R\text{-}EXT}/ R_{ext})*15 \quad （Gain=100\%） \quad V_{R\text{-}EXT}=1.24V;$$



Package Outline

(1) SSOP24-P-150-0.64

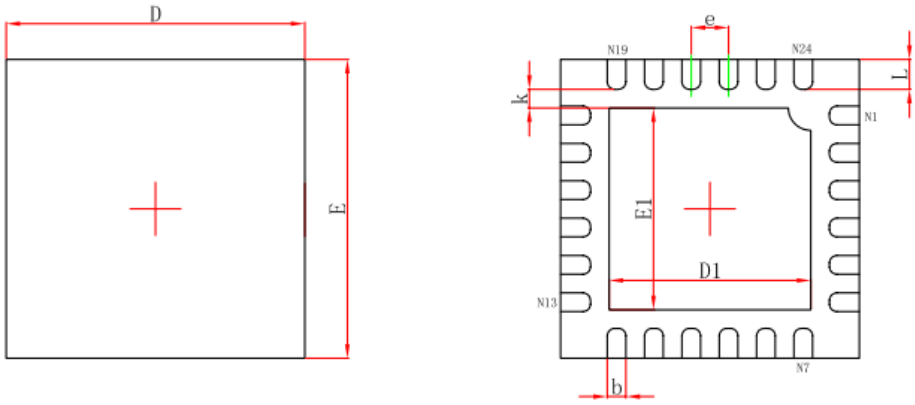
SSOP24 (150mil) PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
A	——	1.750	——	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	——	0.049	——
b	0.203	0.305	0.008	0.012
c	0.102	0.254	0.004	0.010
D	8.450	8.850	0.333	0.348
E1	3.800	4.000	0.150	0.157
E	5.800	6.200	0.228	0.244
e	0.635(BSC)		0.025(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

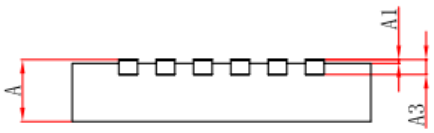
（2）QFN24-4*4-0.5

QFNWB4×4-24L(P0.50T0.75/0.85) PACKAGE OUTLINE DIMENSIONS



Top View

Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	3.924	4.076	0.154	0.160
E	3.924	4.076	0.154	0.160
D1	2.600	2.800	0.102	0.110
E1	2.600	2.800	0.102	0.110
k	0.200MIN.		0.008MIN.	
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.324	0.476	0.013	0.019

Product Ordering Information

Product number	Package （Pb-Free）	Weight（mg）
ICND2038S	SSOP24-P-150-0.635	130
ICND2038SGN-01	QFN24-4*4-0.5	38
ICND2038SGN-02	QFN24-4*4-0.5	38

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