CHIPONE

集创北方

ICND2049

(16-Channel Constant Current LED Driver with Dual Latch and Low Knee Voltage)

Description

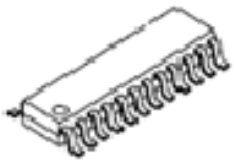
The ICND2049 is a 16-channel constant current output LED driver. All 16-channels constant current can be set by a single external resistor, which provides users flexibility in controlling the light intensity of LEDs.

The ICND2049 exploits current precision controlling technology , which makes error between ICs less than ±2.0%, and error between channels less than ± 2.0%. At ICND2049 output stage , 16-regulated output ports are designed to provide uniform and constant current for driving LEDs within a large range of forward voltage(VF) variations.

ICND2049 contains two 16-bit shift registers and latches which convert serial input data into parallel output format. For integrated dual latches, ICND2049 could get higher refresh rate.

Package

Shrink SOP



AP：SSOP24-150-0.635

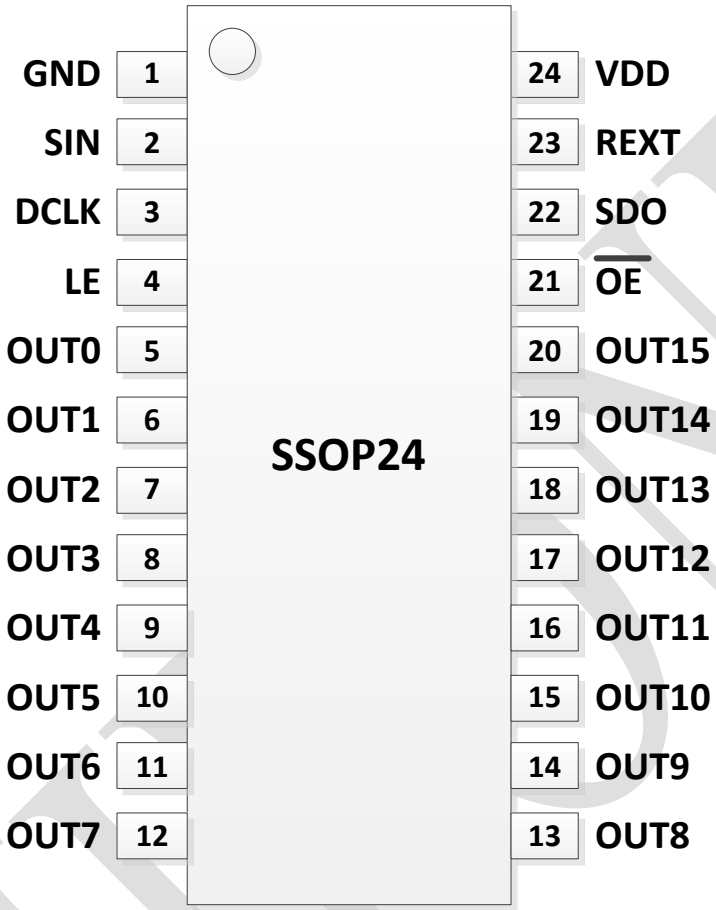
ICND2049

Features

- ✧ 16-channel constant current output
- ✧ Output current setting range:
  0.5~25mA×16@V_{DD}=5V,V_{DS} =0.3V
  0.5~20mA×16@V_{DD}=3.8V,V_{DS} =0.3V
  0.5~15mA×16@V_{DD}=2.8V,V_{DS} =0.45V
- ✧ Current accuracy
  Between channel :< ±2.0%
  Between ICs :< ± 2.0%
- ✧ Fast response of output current:
  $\overline{OE}$ (min):40ns@V_{DD}=5V
- ✧ I/O: Schmitt trigger input
- ✧ Data transfer frequency :f_{MAX}=25MHz(Max)
- ✧ Power supply voltage: V_{DD}=2.6 ~ 5V
- ✧ Operating Temperature: –40°C to +85°C
- ✧ 4 bit current gain：25%~100%
- ✧ LED Open detection
- ✧ Adjustable Pre-Charge for Ghosting Reduction
- ✧ LED Protection Circuit
- ✧ Low-Gray Scale Enhancement
- ✧ Integrated Dual Latches for higher refresh rate
- ✧ Dim line at the first scan line

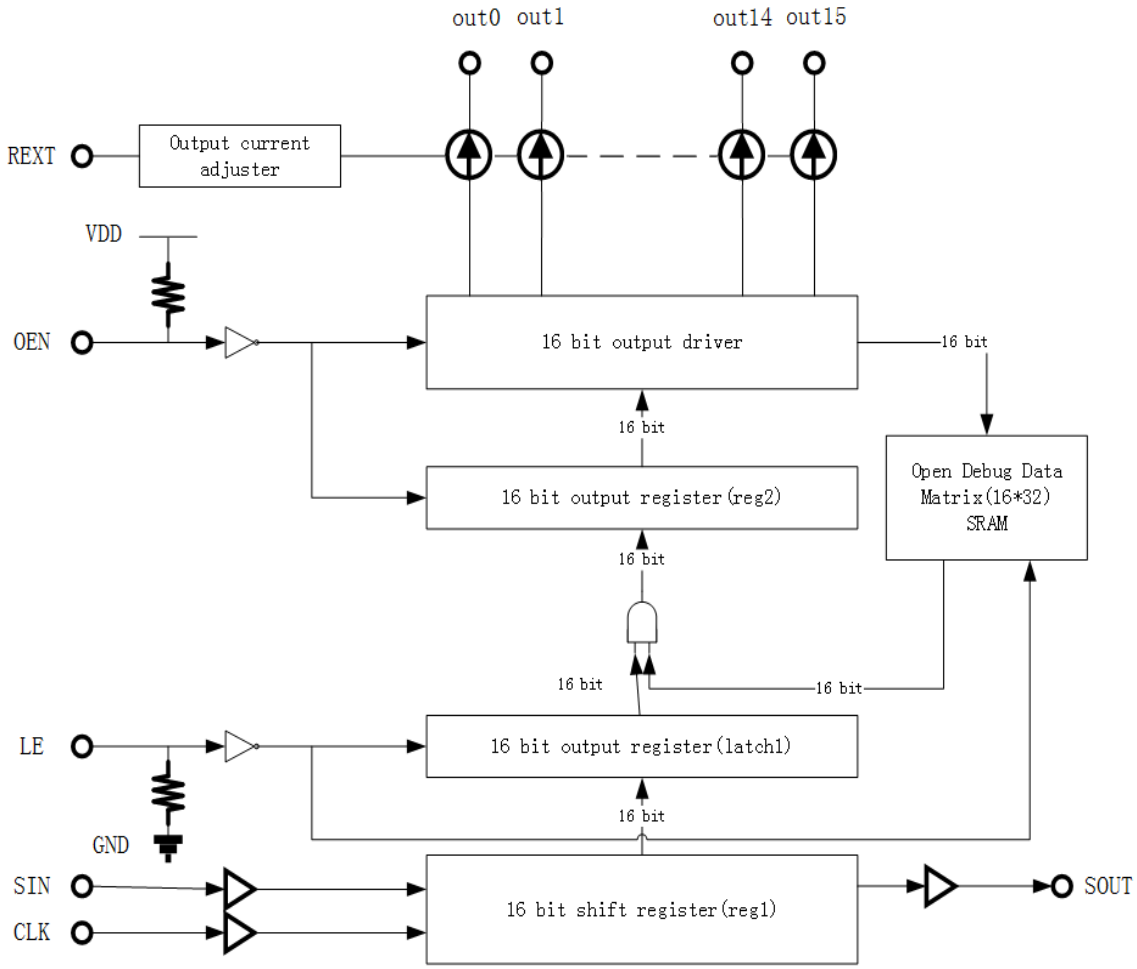
Pin Configuration

AP： SSOP24-P-150-0.635



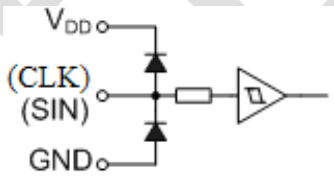
ICND2049 (SSOP24)		
Pin No.	**Pin Name**	**Function**
1	GND	Power Ground
2	SIN	Serial data or command input for driver control
3	CLK	Clock input terminal for data shift on rising edge
4	LE	The command parser is a counter of LE length: A different length of LE indicates a different command.
5～20	OUT0~OUT15	Constant current output
21	$\overline{OE}$	Output enable terminal, $\overline{OE}$ high level, all output drivers are enabled; $\overline{OE}$ low level, all output drivers are turned OFF
22	SOUT	Serial-data or command output to the following IC.
23	R-EXT	Constant-current value setting .Connection to an external resistor to GND.
24	VDD	Power-supply voltage

ICND2049 Block Diagram

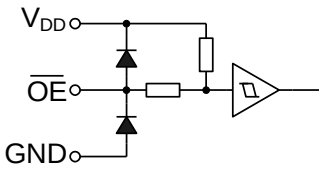


I/O Equivalent Circuits

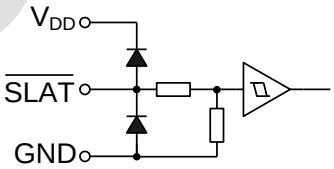
1. CLK, SIN



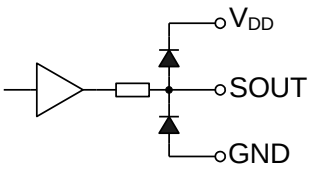
2. $\overline{OE}$



3. LE



4. SOUT



Shift-Register and Command Parser

A simple 16bit shift-register is integrated. All data, such as gray scale and configuration, are latched by the shift-register.

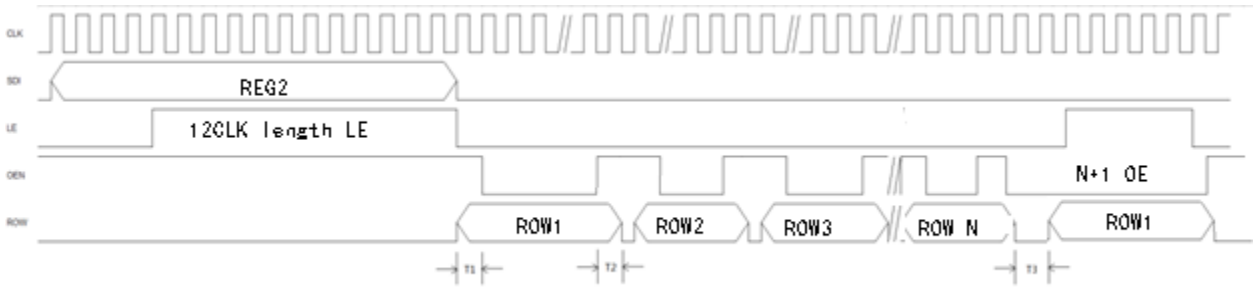
The command parser is a counter of LE length: A different length of LE indicates a different command. Such as a 3bit LE is a “Data Latch” command which indicates that there is a gray scale written in. It will send the 16bit data on shift-register to SRAM.

Control Command

Command Name	Number of DCLK Rising Edge when LE is High	Description
Reset	0	Register is reset to default value.
DATA_LATCH	3	Normal data latch, no line change
	4	Data latch for line change, line number+1
	5	Data latch for the first line
--	6~10	Reserved
WR_REG1	11	Write Configuration Register 1
WR_REG2	12	Write Configuration Register 2

Note1：The length of LE is defined as this: How many positive-edges of DCLK when LE stays logic “1”. For example, the first pulse of LE in the next figure is show a length of 3, which is a “Normal Data Latch” command.

LED Open Detection



1 REG1<10:7>=4'h0000;//Current gain change to 25%
Send REG2 <12:11>=2'h00;//Clear Open detection data
Send REG2 <12:11>=2'h01;//Execute LED open detection

2 Line scan signal change to the first line，Continuously send N+1OE open signal (N for scan number), suggest OE open time greater than 200uS.Sane line changes with OE, for the last OE, scan number back to the first line.

3 During the last OE,send 5 CLK length LE for the Open Detection End.

4 Send REG1 to before setting;// Recovery of current gain
Send REG2 <12:11>=2'h11;//End detection and enable Open LED remove function

NOTE：

1 T1, T2 and T3 require at least 1 CLK clock lengths;

2 Under normal display, the first line needs to use 5 CLK lengths LE, the rest of the non-newline data uses 3 CLK lengths LE, and the newline data uses 4 CLK lengths LE.

Register

Reg1

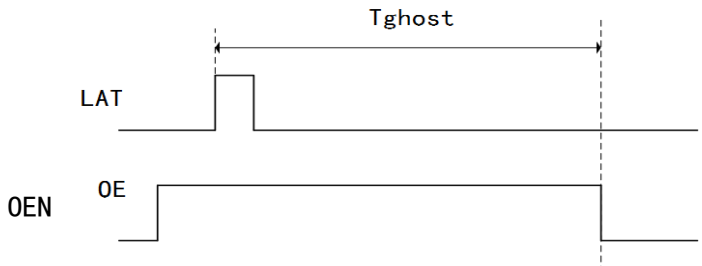
BIT（R1）	NAME	Default	Description
<15:11>	R_UP	5'h1f	Pre-Charge adjust：
<10:7>	R_IGAIN	4'hf	Current Gain：25%~100% 0000~0110：IOUT=IOUT*(25%+<10:7>*3.125%) 0111~1111：IOUT=IOUT*(50%+(<10:7>-7)*6.25%)
<6:4>	Test	3'h7	
<3:0>	Reserved	--	

Reg2

BIT（R2）	NAME	Default	Description
<15:13>	Reserved	3'h0	
<12：11>	OPEN_D	2'h0	LED Open Detection(LOD) Enable 2'h00, 2'h10：LOD disable 2'h01:Execute LOD，refresh data 2'h11:Enable Open LED remove function
<10:9>	Reserved	2'h0	
<8>	R_UPCTRL	1'h0	Ghosting Reduction Enable
<7>	Reserved	--	
<6>	R_LATCH	1'h0	LATCH Select
<5>	R_UPCH	1'h0	Ghosting Reduction Control
<4>	Reserved	1'h0	
<3>	ROUT2<3>	1'h0	Ghosting Reduction Control
<2>	Reserved	--	
<1:0>	R_OE<1:0>	2'h0	OE wider

Ghosting Reduction Waveform

Ghosting Reduction (Tghost) is shown in the figure below. When the OE signal is high, the time between the rising edge of the latch signal (LAT) and the falling edge of the enable signal (OEN) is the extinction time. (Reg2 bit[8]=0 时)



Ghosting Reduction Reg Setting

Reg2 bit[8]/bit[5]/bit[3]

Normal Mode:

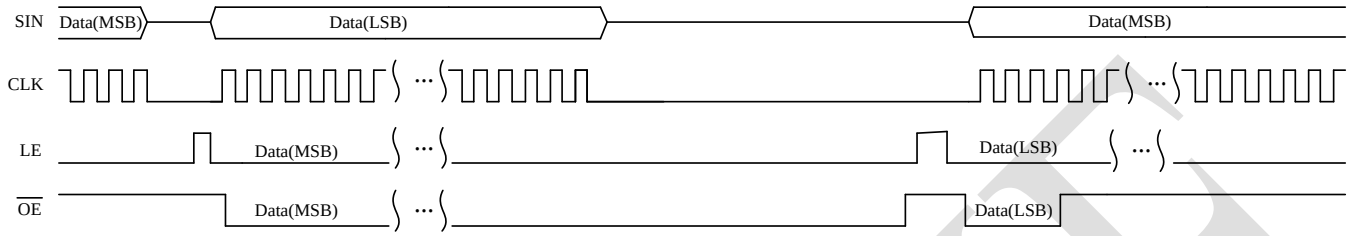
R: Reg2 bit [8/5/3] = 010
G: Reg2 bit [8/5/3] = 010
B: Reg2 bit [8/5/3] = 010

Enhance Mode：

R: Reg2 bit [8/5/3] = 111
G: Reg2 bit [8/5/3] = 111
B: Reg2 bit [8/5/3] = 111

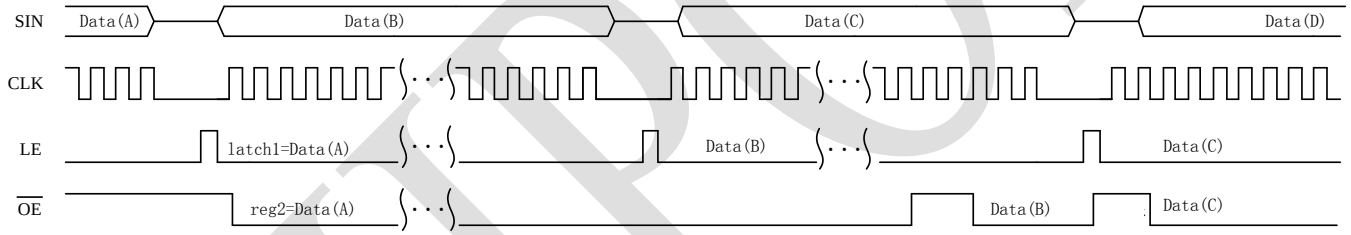
Dual Latch for higher refresh rate

Usual constant current LED driver timing diagrams



1. When display a high bit data, display time may far longer than data transfer time, next data transfer should wait display over.
2. When display a low bit data, display time may far shorter than data transfer time, next display should wait data transfer over.

ICND2049 dual latch timing diagrams



ICND2049 dual latch timing diagrams, data (A) and data (C) are high bit data, data (B) and data (D) are high bit data. Use the free time of display to transfer date could get higher refresh rate.

1. After data(A) transfer over, LE provide a latch signal，latch data(A)
2. After data(A) latched，$\overline{OE}$ from 1to 0，display data(A)
3. When display data(A)，transfer data(B)
4. After data(B) transfer over, LE provide a latch signal，latch data(B),then transfer data(C)
5. After data(A) displayed ，latch data(B) and display data(B)
6. After data(A) transfer over，finish display data(B)
7. Latch data(C) and transfer data(D)

Maximum Ratings (T_a =25℃)

Characteristics		Symbol	Rating	Unit
Supply Voltage		V_{DD}	0~7	V
Output Current		I_O	45	mA
Input Voltage		V_{IN}	−0.4~V_{DD}+0.4	V
Output voltage		V_{OUT}	10V	
Clock Frequency		F_{CLK}	25	MHz
GND Terminal Current		I_{GND}	+1000	mA
Power Dissipation (On PCB，25℃)	DN-type	P_D	3.19	W
Thermal Resistance	DN-type	$R_{th(j-a)}$	39.15	℃/W
Operating Temperature		T_{opr}	−40 ~ 85	℃
Storage Temperature		T_{stg}	−55 ~ 150	℃

DC Items (Unless otherwise specified, T_a =-40℃~85℃)

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	−	2.6	5	5.5	V
High level logic input voltage	V_{IH}	−	0.7*V_{DD}	−	V_{DD}	V
Low level logic input voltage	V_{IL}	−	GND	−	0.3*V_{DD}	V
SOUT high level output Current	I_{OH}	V_{DD}=5V	−	−	−1	mA
SOUT low level output Current	I_{OL}	V_{DD}=5V	−	−	1	mA
Constant current output	I_O	OUT	0.5	−	45	mA

Electrical Characteristics (Unless otherwise specified, V_{DD} =4.5~5.5V，T_a =25℃)

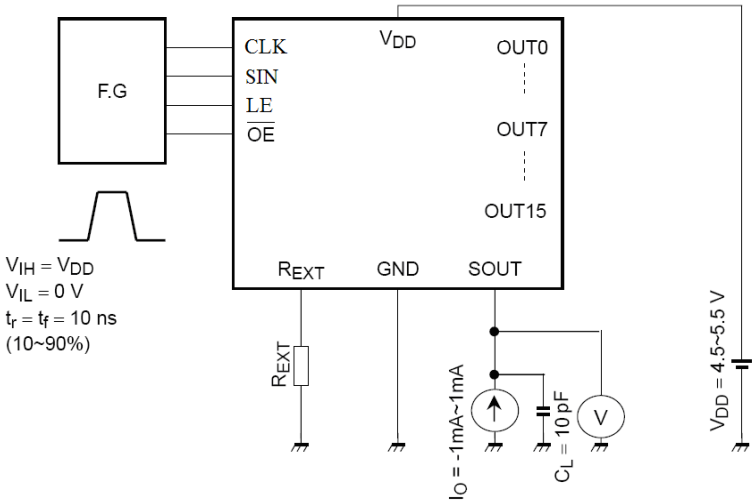
Characteristics	Symbol	Test circuit	Test Conditions	Min	Typ	Max	Unit
High level logic output voltage	V_{OH}	1	I_{OH}=-1mA, SOUT	V_{DD}-0.4	-	V_{DD}	V
Low level logic output voltage	V_{OL}	1	I_{OH}=+1mA, SOUT	-	-	0.4	V
High level logic input current	I_{IH}	2	V_{IN}=V_{DD}, $\overline{OE}$, SIN, CLK	-	-	1	μA
Low level logic input circuit	I_{IL}	3	V_{IN}=GND, LE, SIN, CLK	-	-	-1	μA
Power supply current	I_{DD2}	4	Rext=1.24KΩ，OUT off	-	4.8		mA
	I_{DD3}	4	Rext=620Ω, OUT off	-	6.3		mA
	I_{DD4}	4	Rext=1.24KΩ, OUT on	-	5.5		mA
	I_{DD5}	4	Rext=620Ω, OUT on	-	6.6		mA
Constant current output	I_{O1}	5	V_{DD}=5.0V, V_O=1.0V, R_{EXT}=1.23kΩ	-	15	-	mA
Constant current error	ΔI_O	5	V_{DD}=5.0V, V_O=1.0V, R_{EXT}=1.23kΩ,	-	±0.15	±0.37	mA
Constant current power supply voltage regulation	$\%V_{DD}$	5	V_{DD}=4.5~5.5V, V_O=1.0V, R_{EXT}=1.24kΩ,	-	±0.2	-	%/V
Constant current output voltage regulation	$\%V_{OUT}$	5	V_{DD}=5.0V, V_O=1.0~3.0V, R_{EXT}=1.24kΩ,	-	±0.1		%/V
Pull-up resistor	R_{UP}	3	$\overline{OE}$		500		kΩ
Pull-down resistor	R_{DOWN}	2	LE		500		kΩ

Switching Characteristics (Unless otherwise specified, T_a =25℃，V_{DD} =5.0V)

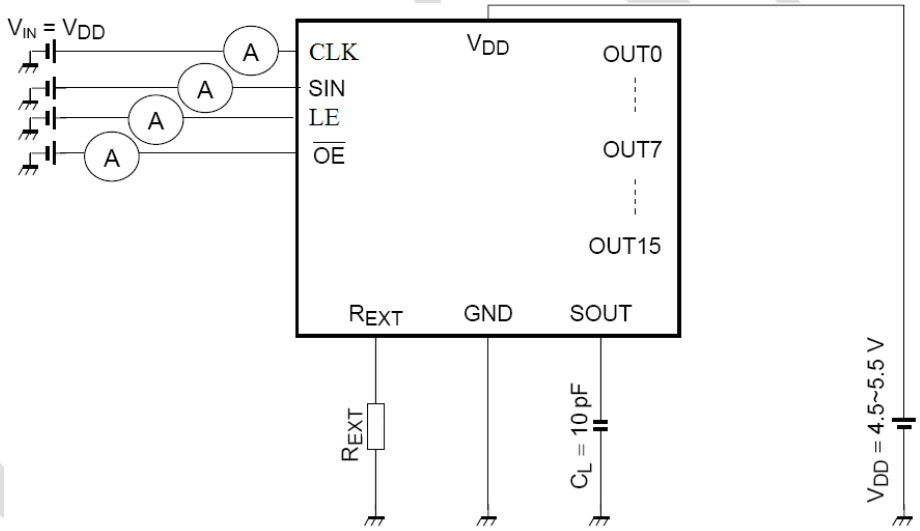
Characteristics		Symbol	Test circuit	Test conditions	Min	Typ	Max	Unit
Propagation delay time	$\overline{OE}$-OUT0	t_{pLH3}	6	LE=H	-	52	-	ns
	$\overline{OE}$-OUT1	t_{pHL3}	6	LE=H	-	31	-	
	CLK-SOUT	t_{pHL}	6	-	-	50%	-	CLK
Output rise time		t_{or}	6	10~90% of voltage waveform	-	38		ns
Output fall time		t_{of}	6	90~10% voltage waveform	-	31		ns

Test Circuit

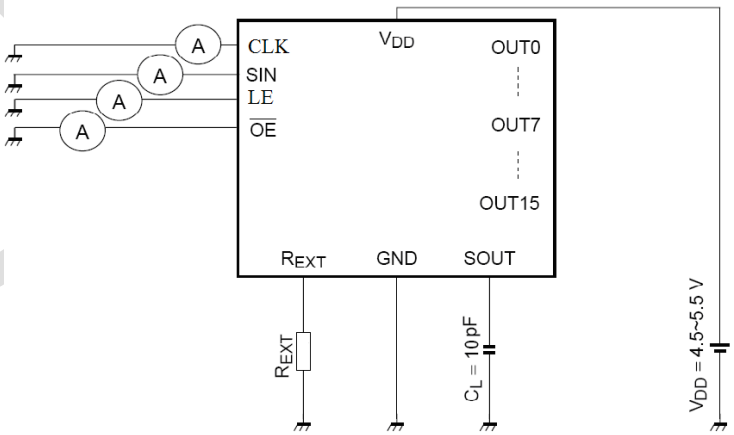
Test Circuit1: High level logic input voltage/Low level logic input voltage



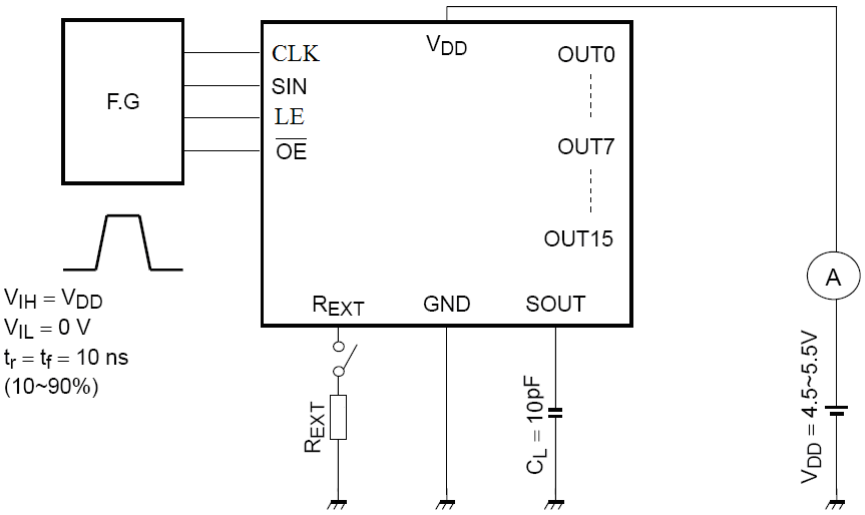
Test Circuit2: High level logic input current/Pull-down resistor



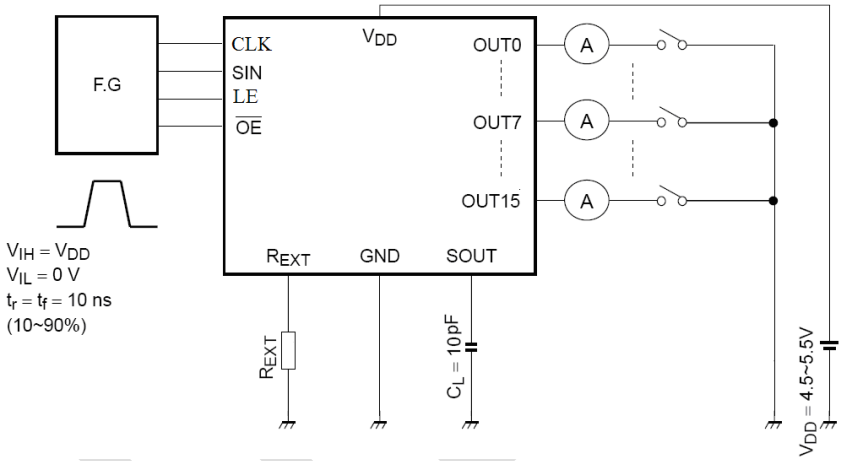
Test Circuit3：Low level logic input current/Pull-up resistor



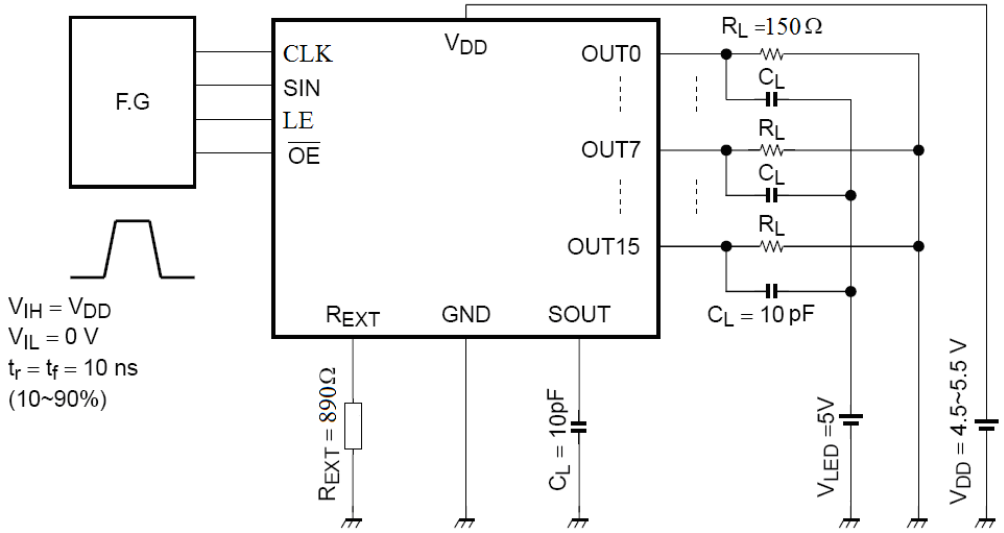
Test Circuit4: Power supply current



Test Circuit5: Constant current output/Output OFF leak current/Constant current error
Constant current power supply voltage regulation/Constant current output voltage regulation



Test Circuit6: Switching Characteristics

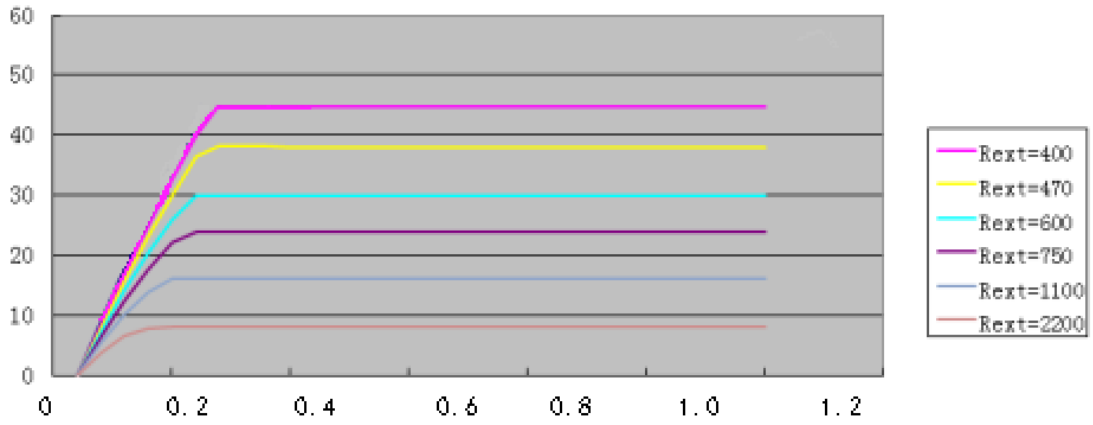


Application Information

ICND2049 exploits current precision controlling technology，and provides nearly no current variations from channel to channel and from IC to IC.

1) The maximum current variation between channels is less than ±2.0%，and that between ICs<±2.0%.

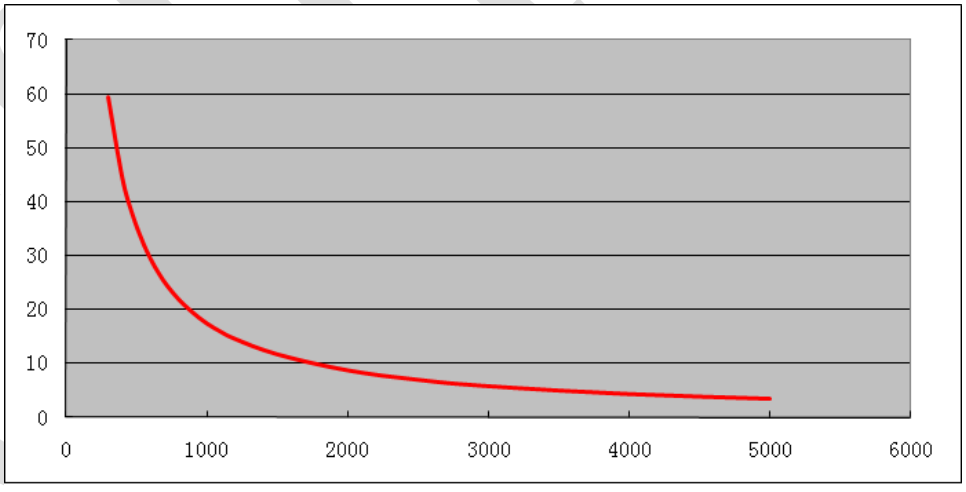
2) The current characteristic of output stage is flat, and can be kept constant regardless of the variations of LED forward voltage.



Setting Output Current

The output current (I_{out}) of ICND2049 is set by an external resistor, R_{ext}. The relationship between I_{out} and R_{ext} is

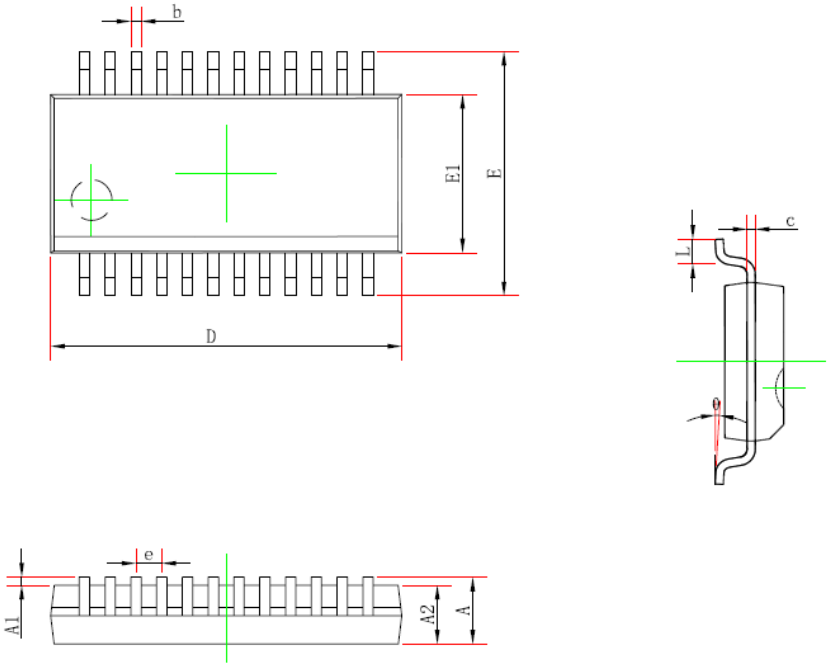
$$Iout=(V_{R\text{-}EXT}/ R_{ext})*15 \quad （Gain=100\%） \quad V_{R\text{-}EXT}=1.24V;$$



Package Outline

AP SSOP24-P-150-0.64

SSOP24 (150mil) PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
A	——	1.750	——	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	——	0.049	——
b	0.203	0.305	0.008	0.012
c	0.102	0.254	0.004	0.010
D	8.450	8.850	0.333	0.348
E1	3.800	4.000	0.150	0.157
E	5.800	6.200	0.228	0.244
e	0.635(BSC)		0.025(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Product Ordering Information

Product number	Package （Pb-Free）	Weight（mg）
ICND2049AP	SSOP24-P-150-0.635	130

Revision History

Rev	Date	Description
1.0	2018/09	Initial Release
1.1	2019/04	Change VDD range
1.2	2019/07	Change Application Information

Important information

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