CHIPONE

集创北方

ICND3018

(16-Channel Power Switch for LED Display)

Description

ICND3018 is a 16-channel power switch for LED display.ICND3018 Integrated 74HC595 (8-bit serial-in, serial parallel-out shift register) and 16 Channel P-Channel Enhancement Mode MOSFET driver.

ICND3018 integrated Ghosting Reduction, Caterpillar Cancelling and LED Protection circuit.

Shrink SOP

AP: SSOP24-P-150-0.635

Quad Flat No-Lead

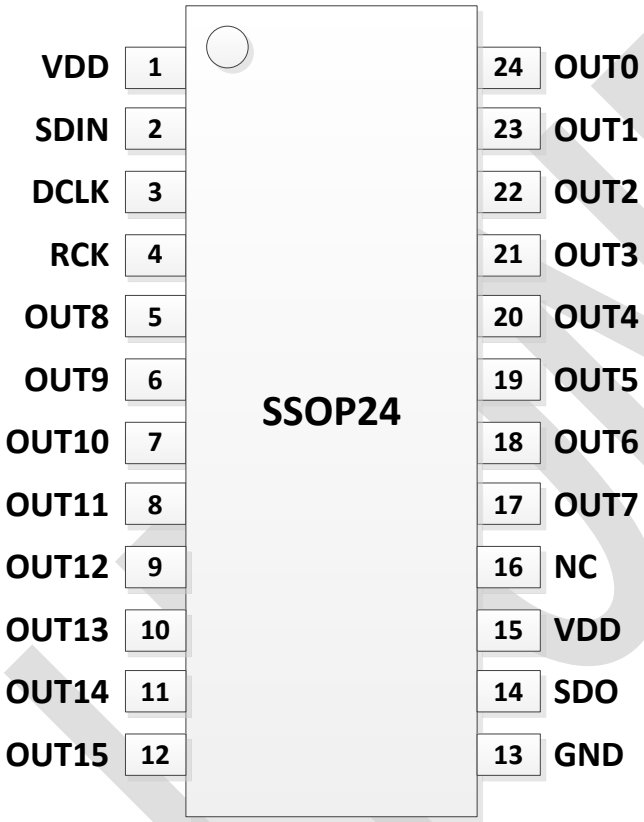
AN: QFN24-4*4-0.5

Features

- ✧ Integrated serial-in, serial parallel-out decoder
- ✧ 16 Channel P-Channel Enhancement Mode MOSFET driver
- ✧ P-MOSTEF $R_{ds(ON)}$ 150 mΩ，Max output current 2A
- ✧ Ghosting Reduction
- ✧ Caterpillar Removal for LED Short
- ✧ LED Protection
- ✧ Up Ghosting Level Adjustable

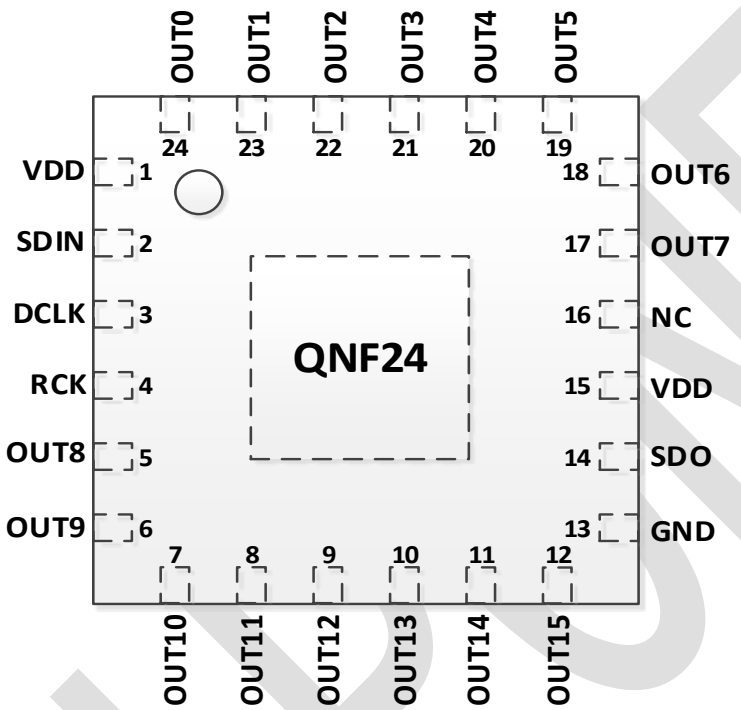
Pin Description

AP：SSOP24



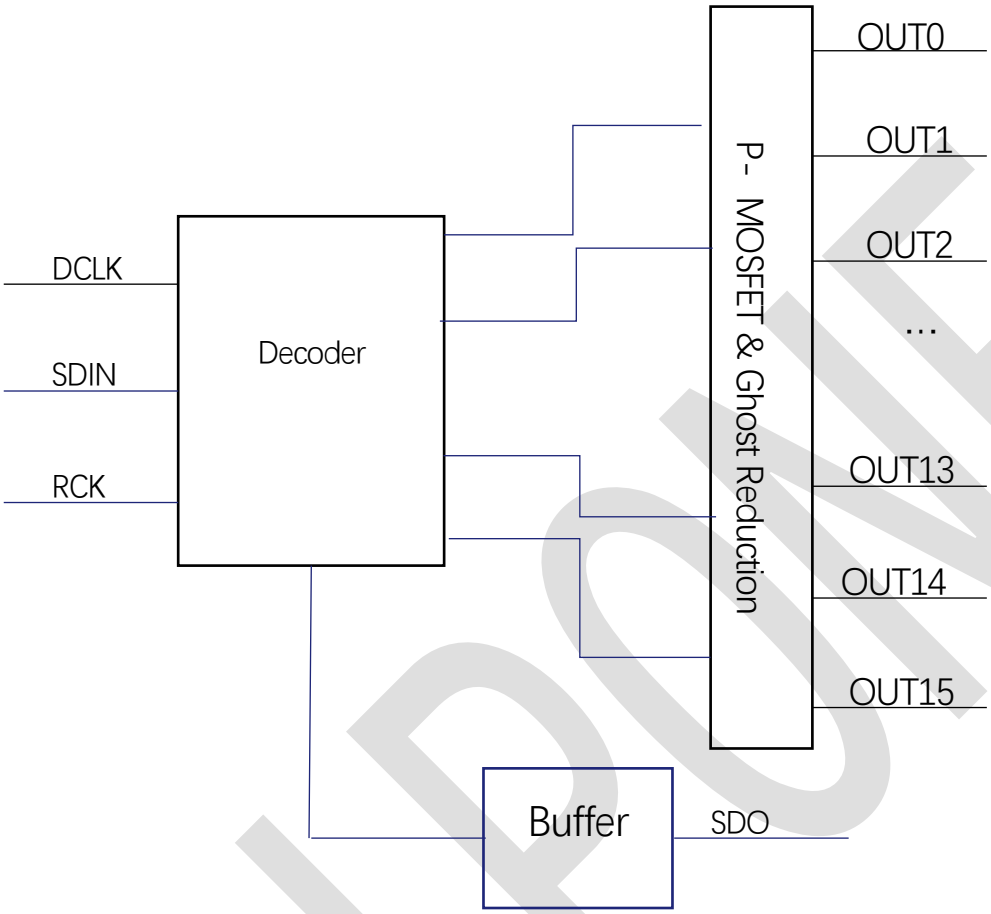
ICND3018AP（SSOP24）		
Pin No	**Pin Name**	**Function**
1，15	VDD	Power-Supply Voltage
2	SDIN	Serial Data Input
3	DCLK	Shift Clock Input
4	RCK	Register Input
5-12 17-24	OUT8-OUT15 OUT7-OUT0	Output with P-Channel Enhancement Mode MOSFET
13	GND	Power Ground
14	SDO	Serial Data Output
16	NC	Not Connected

AN：QFN24-4*4-0.5



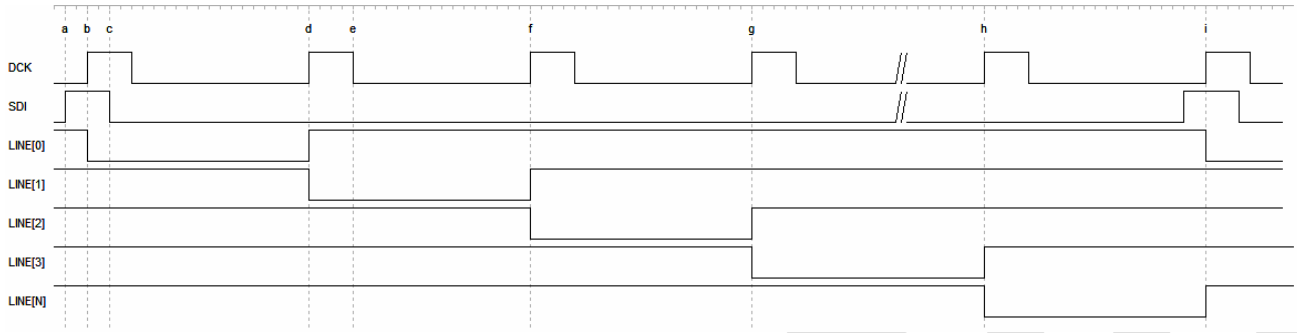
ICND3018AN（QFN24）		
Pin No	**Pin Name**	**Function**
1，15	VDD	Power-Supply Voltage
2	SDIN	Serial Data Input
3	DCLK	Shift Clock Input
4	RCK	Register Input
5-12 17-24	OUT8-OUT15 OUT7-OUT0	Output with P-Channel Enhancement Mode MOSFET
13	GND	Power Ground
14	SDO	Serial Data Output
16,E-pad	NC	Not Connected

Block Diagram



Time Waveform

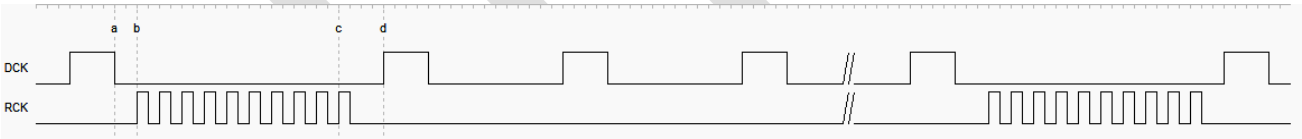
The rising edge of DCLK is a line feed signal. After receiving the rising edge of DCLK, the data is shifted once, and the corresponding open channel is also shifted. The width of DCLK is the elimination time, so we need to do DCLK width and interface elimination parameter linkage.



Time	Function	MIN
Tb-Td	***Display time***， between the two DCLK rising edge	
Te-Tf	***Registers configure time*** **,**the DLCK falling edge to the next rising edge	
Td-Te	***Ghost reduction time***, DCLK pulse width	500ns
Ta-Tb	Setup time	20ns
Tb-Tc	Hold time	20ns

Register Setting

Ta-Td，***Registers configure time,*** the DLCK falling edge to the next rising edge.



Register and Number of RCLK Rising Edge when DCK is Low.

Reg[3:0]=RCLK-8

Time	Function	MIN
Tb-Tc	Register configuration time（Reg[3:0]=RCLK-8）	
Ta-Tb	Register configuration pre blank area	100ns
Tc-Td	Register configuration behind blank area	100ns

Register

Number of RCK Rising Edge when DCLK is Low	Model<3 >	Level <2:0>	Level(V)
8	0	000	N/A
9		001	2.25
10		010	2.5
11		011	2.75
12		100	3.0
13		101	3.25
14		110	3.5
15		111	3.75
16	1	000	N/A
17		001	2.25
18		010	2.5
19		011	2.75
20		100	3.0
21		***101***	***3.25(Default)***
22		110	3.5
23		111	3.75

Default<3:0>=1101

Specifications

Maximum Ratings (T_a =25℃)

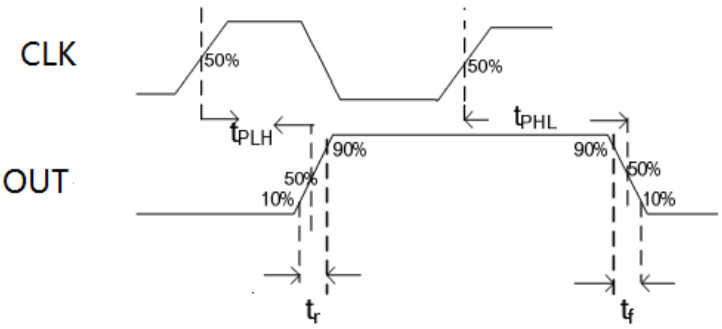
Characteristics	Symbol	Rating	Unit
Supply Voltage	V_{DD}	-0.5 ～ +7.0	V
Input Voltage	VIN	-0.5 ～ VDD+0.5	V
Operating Temperature	Topt	-40 ～ +80	℃
Storage Temperature	Tstg	-50 ～ +150	℃

DC Items (Unless otherwise specified, T_a =-40℃~85℃)

Characteristics	Symbol	Min	Typ	Max	Unit	Test Conditions
Power Supply Voltage	V_{DD}	3.0	5.0	5.5	V	-
High Level Logic Input Voltage	V_{IH}	0.7*V_{DD}	-	-	V	-
High Level Logic Input Voltage	V_{IL}	-	-	0.3*V_{DD}	V	-
Quiescent Device Current	I_{DD}	-	3	-	mA	V_{DD}=5.0V
Drain Current	I_{OH}	-	-	2	A	V_{DD}=5.0V
Drain-Source On-State Resistance	$R_{DS(on)}$	-	150	-	mΩ	V_{DD}=5.0V

Switching Characteristics (Unless otherwise specified, T_a =25℃，V_{DD}=5.0V)

Characteristics	Symbol	Min	Typ	Max	Unit	Test conditions
Propagation	t_{PLH}	-	52	-	nS	V_{DD}=5.0V
Delay Time	t_{PHL}	-	134	-	nS	CL=50pF
Output rise Time	tr	-	19	-	nS	
Output fall Time	tf	-	160	-	nS	



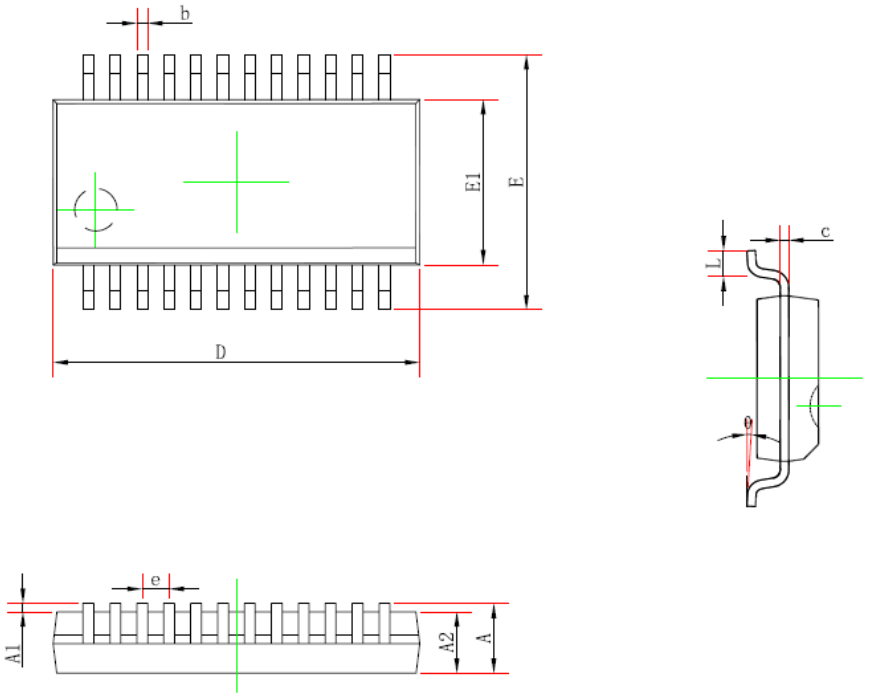
Application Note

1. The channels used must be used in OUT0~OUT15 order
2. No idle channels are available in the number of scanned numbers
3. The initial input data of the scanning group can only be introduced from 245 of the line, and cannot be imported from the output of the last scan group.

Package Outline

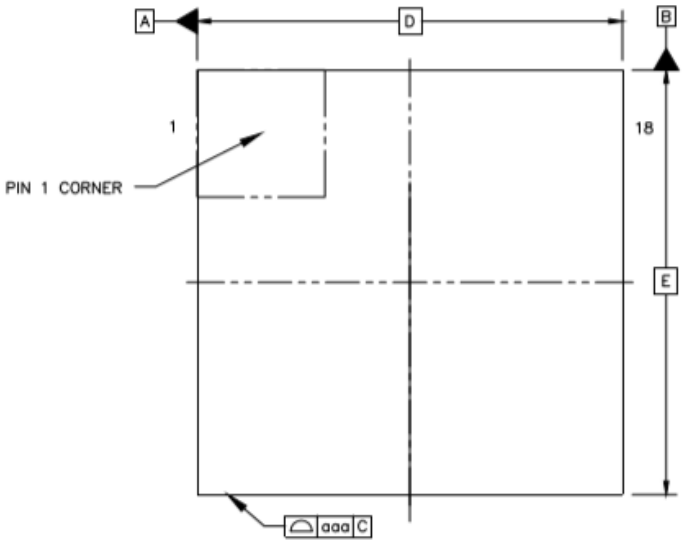
1.SSOP24

SSOP24 (150mil) PACKAGE OUTLINE DIMENSIONS

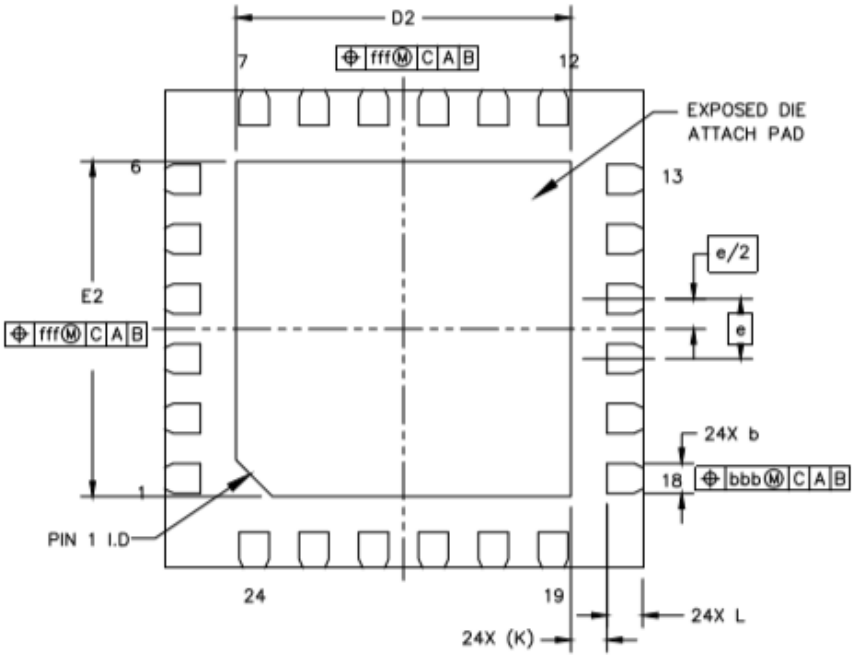


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
A	——	1.750	——	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	——	0.049	——
b	0.203	0.305	0.008	0.012
c	0.102	0.254	0.004	0.010
D	8.450	8.850	0.333	0.348
E1	3.800	4.000	0.150	0.157
E	5.800	6.200	0.228	0.244
e	0.635 (BSC)		0.025 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

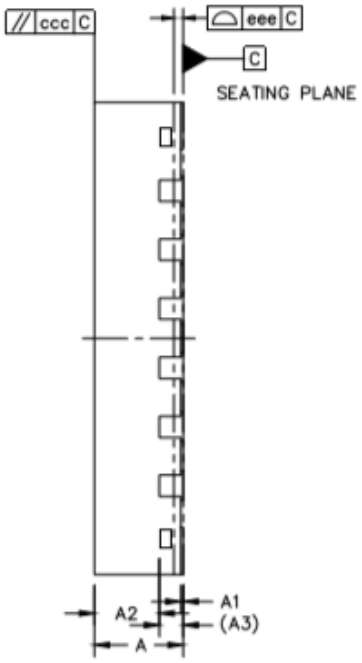
2.QFN24



TOP VIEW



BOTTOM VIEW



SIDE VIEW

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	2.7	2.8	2.9
	Y	E2	2.7	2.8	2.9
LEAD LENGTH		L	0.2	0.3	0.4
LEAD TIP TO EXPOSED PAD EDGE		K		0.3 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	

Product Ordering Information

Product number	Package （Pb-Free）	Pitch (mm)
ICND3018AP	SSOP24	0.635
ICND3018AN	QFN24	0.5

Revision History

Rev	Date	Description
1.0	2019/06	Initial Release
1.1	2020/08	Change Register 4'1000=N.A

Important information

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