



ICND8390

**(16-Channel Constant Current Multi-functional LED Driver with
Error Detection)**

Description

ICND8390 is a 16-channel constant current sink LED driver with comprehensive error detection and power saving features, which make LED display more reliable and energy saving particularly in LED traffic sign and variable message sign applications.

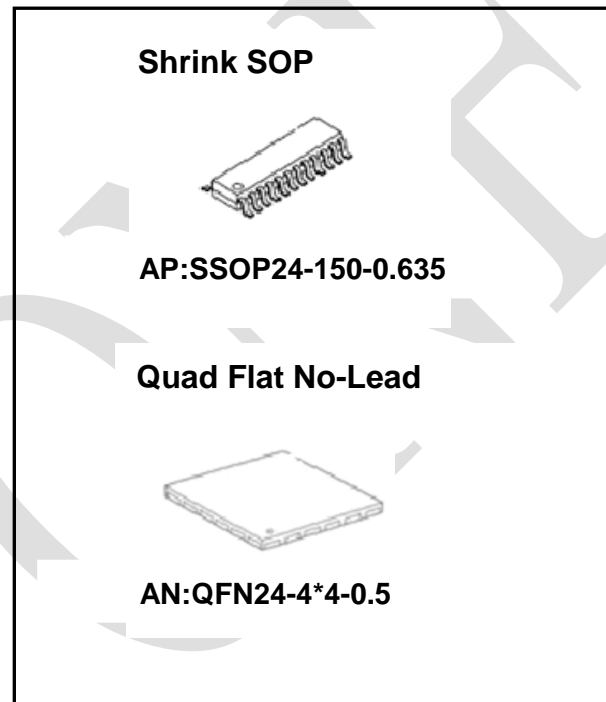
ICND8390 incorporates lower ghosting effect elimination function which can enhance LED display quality in time-multiplexing fine pitch design.

All 16-channel constant current output of ICND8390 can be set by once single external resistor which allows users simply control of LED light intensity. The brightness of LED can be further programmable by internal configuration command of current gain function.

Features

- ✧ 16-channel constant current output
Output current setting range :
8~100mA×16@V_{DD}=5V constant current output
3~80mA×16@V_{DD}=3.3V constant current output
- ✧ Current accuracy
Between channel :< ±2.0%
Between ICs :< ± 2.0%
- ✧ 6 bit current gain: 12.5%~200%
- ✧ Fast response of output current,
 \overline{OE} (min):40ns@V_{DD}=5V
- ✧ I/O: schmitt trigger input
- ✧ Power supply voltage: V_{DD}=3.3 ~ 5V
- ✧ Low knee voltage
I_{OUT}=20mA@V_{DS}=0.2V, V_{DD}=5.0V
- ✧ Data transfer frequency:f_{MAX}=30MHz(Max)
- ✧ Adjustable pre-charge for ghosting reduction
- ✧ Support both compulsory error detection and
In-message error detection
LED open/short detection
LED leakage detection
LED error data return
Next short protection
Over temperature protection
- ✧ Sleep mode support
- ✧ Staggered delay
- ✧ Operating temperature: -40°C to +85°C

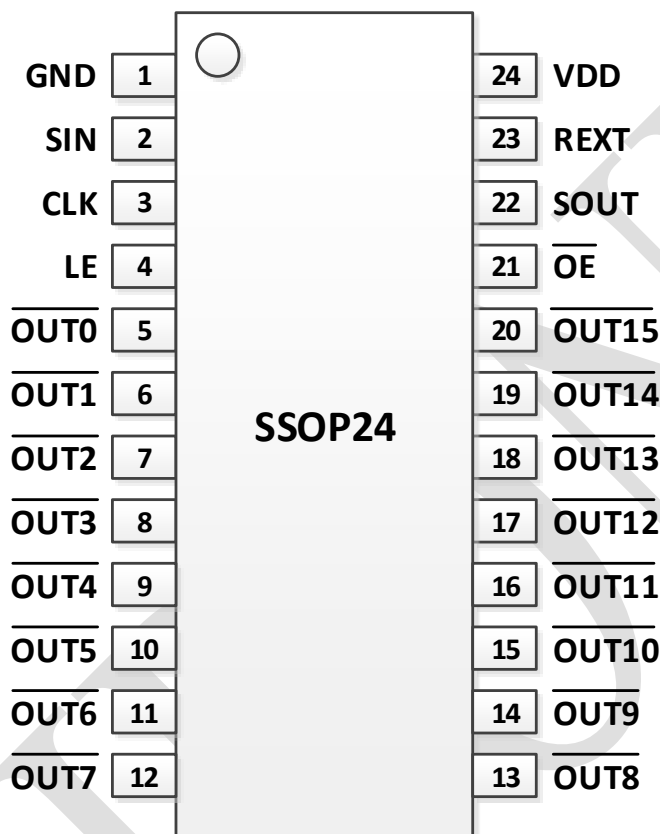
Package



ICND8390

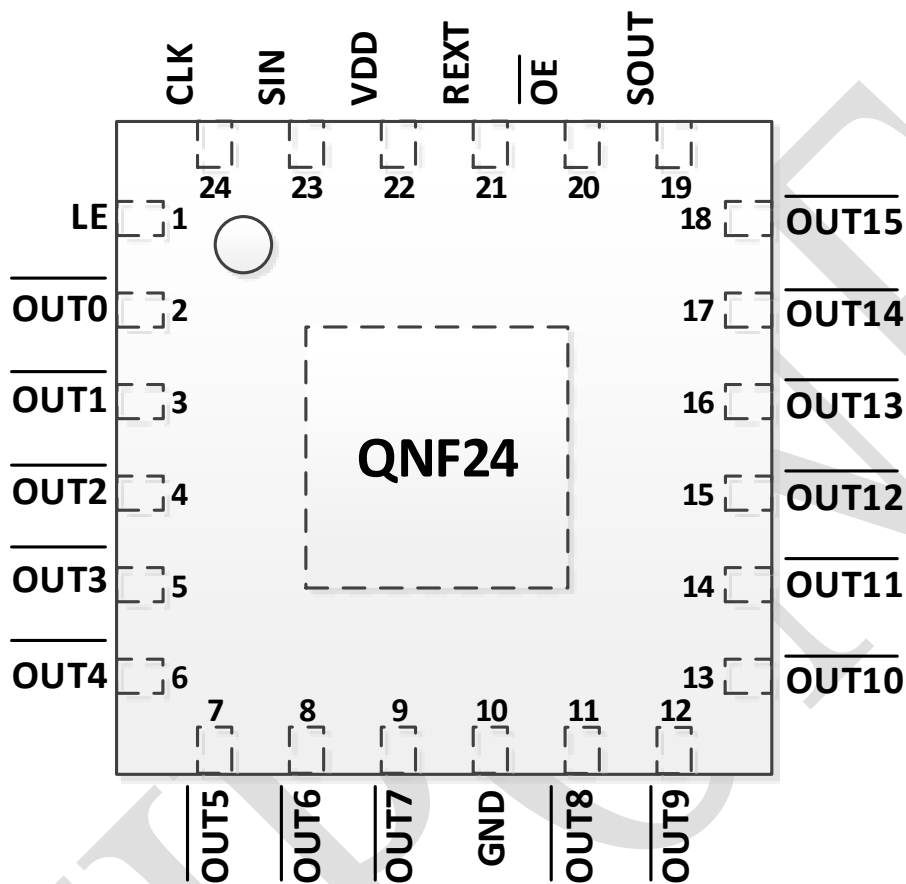
Pin Configuration

SSOP24-P-150-0. 635



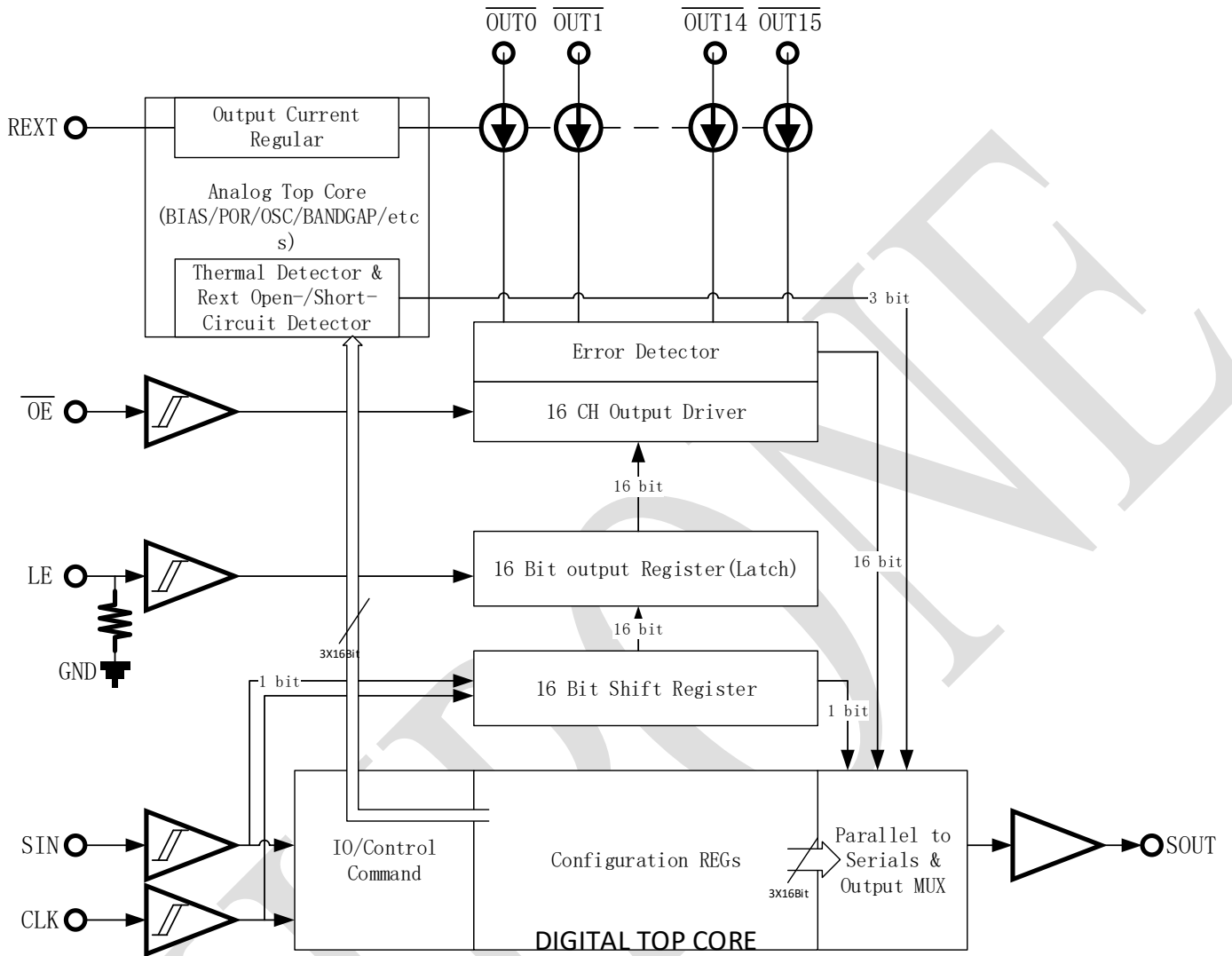
ICND8390AP (SSOP24)		
Pin No.	Pin Name	Function
1	GND	Power Ground
2	SIN	Serial data or command input for driver control
3	CLK	Clock input terminal for data shift on rising edge
4	LE	Data and command latch
5~20	$\overline{\text{OUT0}} \sim \overline{\text{OUT15}}$	Constant current output
21	$\overline{\text{OE}}$	Output enable terminal, $\overline{\text{OE}}$ high level, all output drivers are disabled; $\overline{\text{OE}}$ low level, all output drivers are enabled
22	SOUT	Serial-data or command output to the following IC.
23	R-EXT	Constant-current value setting .Connection to an external resistor to GND.
24	VDD	Power-supply voltage

2 QFN24-4*4-0.5

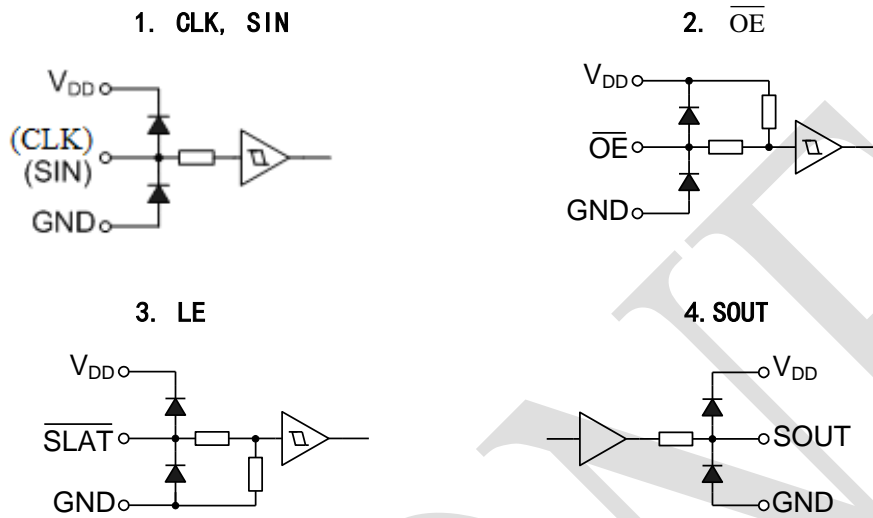


ICND8390AN (QFN24)		
Pin No.	Pin Name	Function
1	LE	The command parser is a counter of LE length: A different length of LE indicates a different command
2~9, 11~18	OUT0 ~ OUT15	Constant current output
10	GND	Power Ground
19	SOUT	Serial-data or command output to the following IC
20	OE	Output enable terminal, OE high level, all output drivers are disabled; OE low level, all output drivers are enabled
21	R-EXT	Constant-current value setting .Connection to an external resistor to GND
22	VDD	Power-supply voltage
23	SIN	Serial data or command input for driver control
24	CLK	Clock input terminal for data shift on rising edge

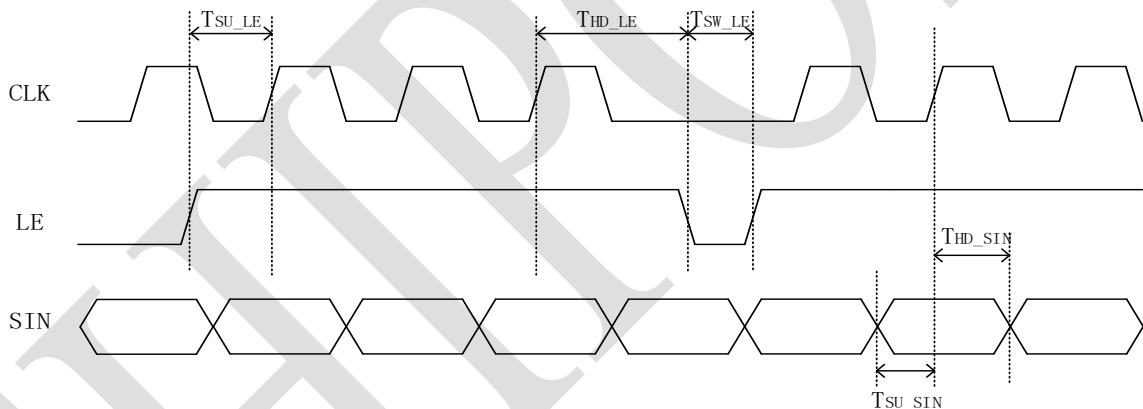
Block Diagram



I/O Equivalent Circuits



LE waveforms



Hold time

Name	MIN	Note
T_{su_LE}	7ns	
T_{hd_LE}	7ns	
T_{sw_LE}	10ns	
T_{su_SIN}	3ns	
T_{hd_SIN} ,	3ns	

Maximum Ratings ($T_a = 25^\circ\text{C}$)

Characteristics		Symbol	Rating	Unit
Supply Voltage		V_{DD}	0~7	V
Output Current		I_o	100	mA
Input Voltage		V_{IN}	$-0.4 \sim V_{DD} + 0.4$	V
Output voltage		V_{OUT}	17V	
Clock Frequency		F_{CLK}	30	MHz
GND Terminal Current		I_{GND}	+1650	mA
Power Dissipation (On 4layer PCB, 25°C)	AN	P_D	4.09	W
	AP		1.98	
Thermal Resistance	AN	$R_{th(j-a)}$	30.5	°C/W
	AP		64	
Operating Temperature		T_{opr}	-40 ~ 85	°C
Storage Temperature		T_{stg}	-55 ~ 150	°C

DC Items (Unless otherwise specified, $T_a = -40^\circ\text{C} \sim 85^\circ\text{C}$)

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	-	3.3	5	6.0	V
Output Voltage when ON	$V_{O(ON)}$	\overline{OUTn}	0.6	-	4	V
High level logic input voltage	V_{IH}	-	$0.7 * V_{DD}$	-	V_{DD}	V
Low level logic input voltage	V_{IL}	-	GND	-	$0.3 * V_{DD}$	V
SOUT high level output Current	I_{OH}	$V_{DD}=5V$	-	-	-1	mA
SOUT low level output Current	I_{OL}	$V_{DD}=5V$	-	-	1	mA
Constant current output	I_o	\overline{OUTn}	3	-	100	mA

Transition Items (Unless otherwise specified, $V_{DD}=3.3V$, $T_a=-40^{\circ}C\sim 85^{\circ}C$)

Characteristics	Symbol	Test circuit	Test Conditions	Min	Typ	Max	Unit
Serial data transfer frequency	F_{CLK}	6	-	-	-	25	MHz
Clock pulse width	t_{wCLK}	6	SCK=H or L	20	-	-	ns
Latch pulse width	t_{wLE}	6	LE=H	20	-	-	ns
Enable pulse width	t_{wOE}	6	$\overline{OE}=H$ or L, $R_{EXT}=890\Omega$	40	-	-	ns
Hold time	t_{HOLD1}	6	-	5	-	-	ns
	t_{HOLD2}	6	-	5	-	-	ns
Setup time	t_{SETUP1}	6	-	5	-	-	ns
	t_{SETUP2}	6	-	5	-	-	ns
Maximum clock rise time	t_r	6	-	-	-	500	ns
Maximum clock fall time	t_f	6	-	-	-	500	ns

Transition Items (Unless otherwise specified, $V_{DD}=5V$, $T_a=-40^{\circ}C\sim 85^{\circ}C$)

Characteristics	Symbol	Test circuit	Test Conditions	Min	Typ	Max	Unit
Serial data transfer frequency	F_{CLK}	6	-	-	-	30	MHz
Clock pulse width	t_{wCLK}	6	SCK=H or L	20	-	-	ns
Latch pulse width	t_{wLE}	6	LE=H	20	-	-	ns
Enable pulse width	t_{wOE}	6	$\overline{OE}=H$ or L, $R_{EXT}=890\Omega$	40	-	-	ns
Hold time	t_{HOLD1}	6	-	5	-	-	ns
	t_{HOLD2}	6	-	5	-	-	ns
Setup time	t_{SETUP1}	6	-	5	-	-	ns
	t_{SETUP2}	6	-	5	-	-	ns
Maximum clock rise time	t_r	6	-	-	-	500	ns
Maximum clock fall time	t_f	6	-	-	-	500	ns

Electrical Characteristics (Unless otherwise specified, $V_{DD}=3.3V$, $T_a=25^{\circ}C$)

Characteristics	Symbol	Test circuit	Test Conditions	Min	Typ	Max	Unit
High level logic output voltage	V_{OH}	1	$I_{OH}=-1mA$, SOUT	$V_{DD}-0.4$	-	V_{DD}	V
Low level logic output voltage	V_{OL}	1	$I_{OH}=+1mA$, SOUT	-	-	0.4	V
High level logic input current	I_{IH}	2	$V_{IN}=V_{DD}$, \overline{OE} , SIN, CLK	-	-	1	μA
Low level logic input circuit	I_{IL}	3	$V_{IN}=GND$, LE, SIN, CLK	-	-	-1	μA
Power supply current	I_{DD1}	4	OUT off, Saving ON	-	18	-	μA
	I_{DD2}	4	$R_{ext}=10K\Omega$, OUT off	-	1.6	-	mA
	I_{DD3}	4	$R_{ext}=1K\Omega$, OUT off	-	5.0	-	mA

	I_{DD4}	4	$R_{EXT}=10K\Omega$, OUT on	-	1.5	-	mA
	I_{DD5}	4	$R_{EXT}=1K\Omega$, OUT on	-	5.1	-	mA
Constant current error	ΔI_o	5	$I_{OUT}=15mA$	-	± 0.17	± 0.30	mA
Constant current power supply voltage regulation	$\%V_{DD}$	5	$V_{DD}=3\sim 3.6V$, $V_o=1.0V$, $R_{EXT}=1.24k\Omega$, $\frac{OUT0}{OUT0} \sim \frac{OUT15}{OUT15}$	-	± 0.3	-	%/V
Constant current output voltage regulation	$\%V_{OUT}$	5	$V_{DD}=3.3V$, $V_o=1.0\sim 2.0V$, $R_{EXT}=1.24k\Omega$, $\frac{OUT0}{OUT0} \sim \frac{OUT15}{OUT15}$	-	± 0.2	-	%/V
Pull-up resistor	R_{UP}	3	\overline{OE}	250	500	800	k Ω
Pull-down resistor	R_{DOWN}	2	LE	250	500	800	k Ω

Electrical Characteristics (Unless otherwise specified, $V_{DD}=5V$, $T_a=25^\circ C$)

Characteristics	Symbol	Test circuit	Test Conditions	Min	Typ	Max	Unit
High level logic output voltage	V_{OH}	1	$I_{OH}=-1mA$, SOUT	$V_{DD}-0.4$	-	V_{DD}	V
Low level logic output voltage	V_{OL}	1	$I_{OH}=+1mA$, SOUT	-	-	0.4	V
High level logic input current	I_{IH}	2	$V_{IN}=V_{DD}$, \overline{OE} , SIN, CLK	-	-	1	μA
Low level logic input circuit	I_{IL}	3	$V_{IN}=GND$, LE, SIN, CLK	-	-	-1	μA
Power supply current	I_{DD1}	4	OUT off, Saving ON	-	17	-	μA
	I_{DD2}	4	$R_{EXT}=10K\Omega$, OUT off	-	1.4	-	mA
	I_{DD3}	4	$R_{EXT}=1K\Omega$, OUT off	-	4.8	-	mA
	I_{DD4}	4	$R_{EXT}=10K\Omega$, OUT on	-	1.4	-	mA
	I_{DD5}	4	$R_{EXT}=1K\Omega$, OUT on	-	4.9	-	mA
Constant current error	ΔI_o	5	$I_{OUT}=15mA$	-	± 0.17	± 0.30	mA
Constant current power supply voltage regulation	$\%V_{DD}$	5	$V_{DD}=4.5\sim 5.5V$, $V_o=1.0V$, $R_{EXT}=1.24k\Omega$, $\frac{OUT0}{OUT0} \sim \frac{OUT15}{OUT15}$	-	± 0.3	-	%/V
Constant current output voltage regulation	$\%V_{OUT}$	5	$V_{DD}=5.0V$, $V_o=1.0\sim 3.0V$, $R_{EXT}=1.24k\Omega$, $\frac{OUT0}{OUT0} \sim \frac{OUT15}{OUT15}$	-	± 0.2	-	%/V
Pull-up resistor	R_{UP}	3	\overline{OE}	250	500	800	k Ω
Pull-down resistor	R_{DOWN}	2	LE	250	500	800	k Ω

Switching Characteristics (Unless otherwise specified, $V_{DD} = 3.3V$, $T_a = 25^\circ C$)

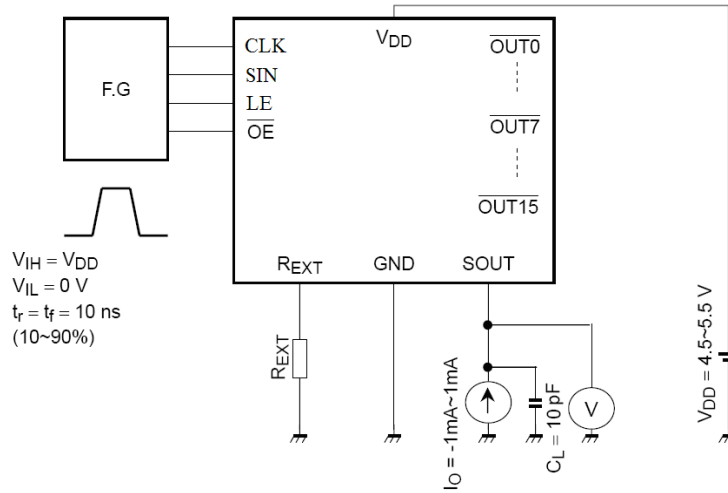
Characteristics		Symbol	Test circuit	Test conditions	Min	Typ	Max	Unit
Propagation delay time	$\overline{OE} - \overline{OUT0}$	t_{pLH3}	6	LE=H	-	71	-	ns
	$\overline{OE} - \overline{OUT1}$	t_{pHL3}	6	LE=H	-	69	-	
	CLK-SOUT	t_{pHL}	6	-	-	23	-	
Output rise time		t_{or}	6	10~90% of voltage waveform	-	48	-	ns
Output fall time		t_{of}	6	90~10% voltage waveform	-	37	-	ns

Switching Characteristics (Unless otherwise specified, $V_{DD} = 5.0V$, $T_a = 25^\circ C$)

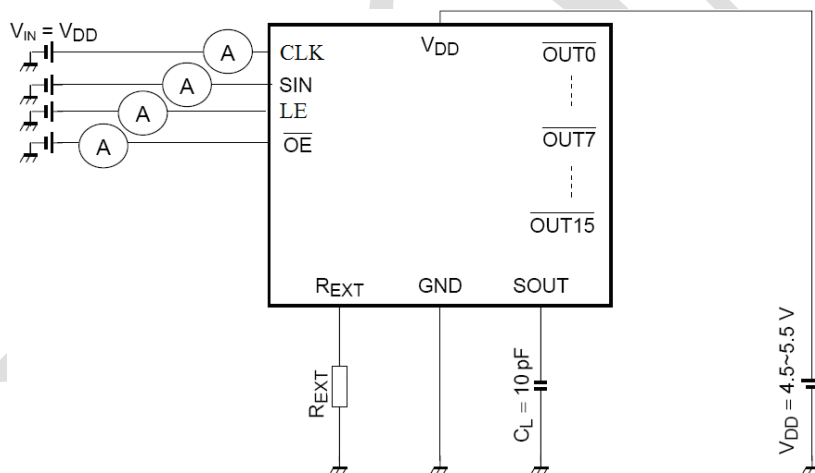
Characteristics		Symbol	Test circuit	Test conditions	Min	Typ	Max	Unit
Propagation delay time	$\overline{OE} - \overline{OUT0}$	t_{pLH3}	6	LE=H	-	65	-	ns
	$\overline{OE} - \overline{OUT1}$	t_{pHL3}	6	LE=H	-	68	-	
	CLK-SOUT	t_{pHL}	6	-	-	21	-	
Output rise time		t_{or}	6	10~90% of voltage waveform	-	55	-	ns
Output fall time		t_{of}	6	90~10% voltage waveform	-	45	-	ns

Test Circuit

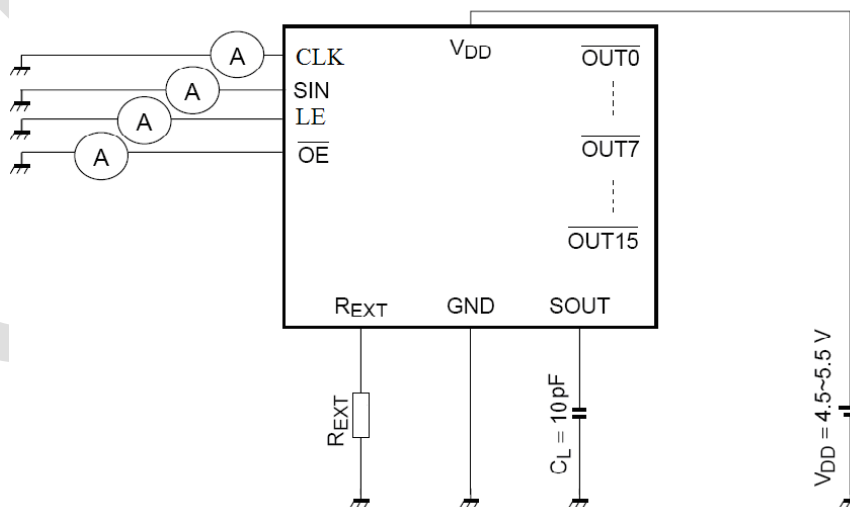
Test Circuit1: High level logic input voltage/Low level logic input voltage



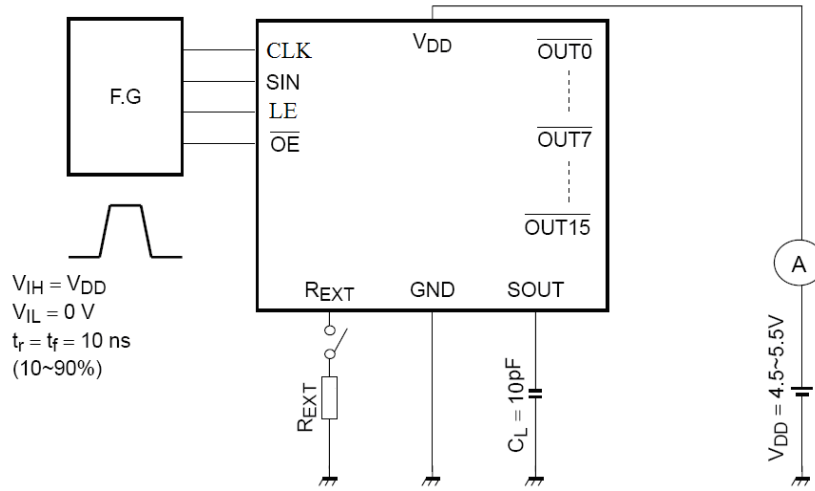
Test Circuit2: High level logic input current/Pull-down resistor



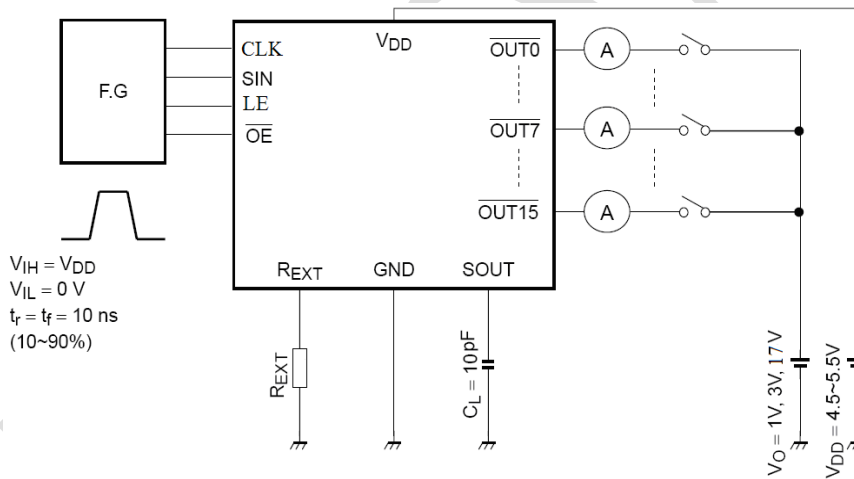
Test Circuit3: Low level logic input current/Pull-up resistor



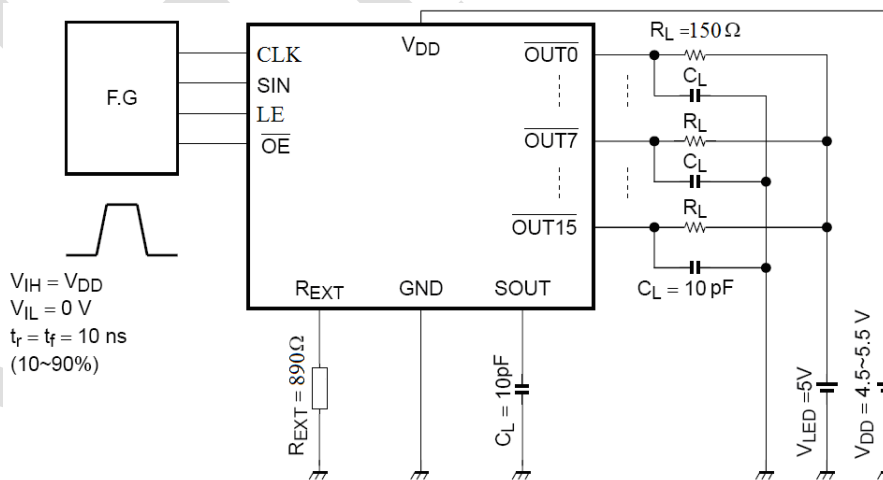
Test Circuit4: Power supply current



**Test Circuit5: Constant current output/Output OFF leak current/Constant current error
Constant current power supply voltage regulation/Constant current output voltage regulation**

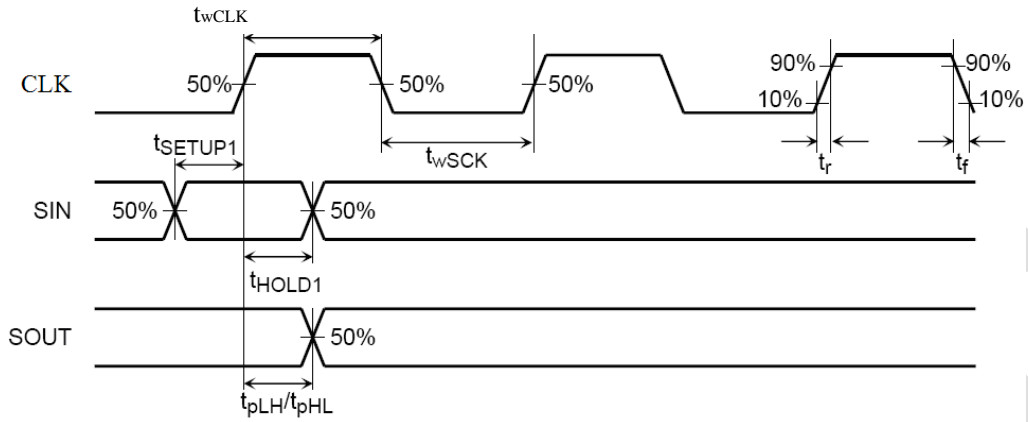


Test Circuit6: Switching Characteristics

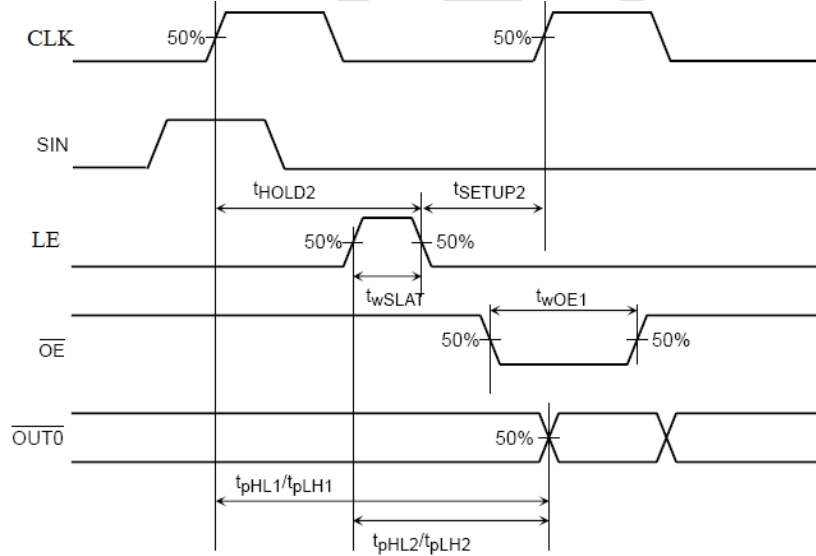


Timing Waveforms

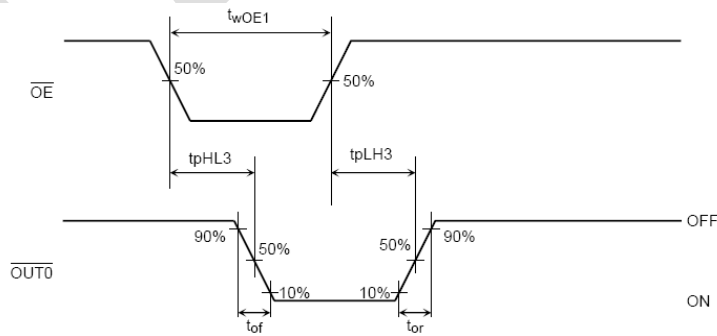
1. CLK, SIN, SOUT



2. CLK, SIN, LE, \overline{OE} , $\overline{OUT0}$



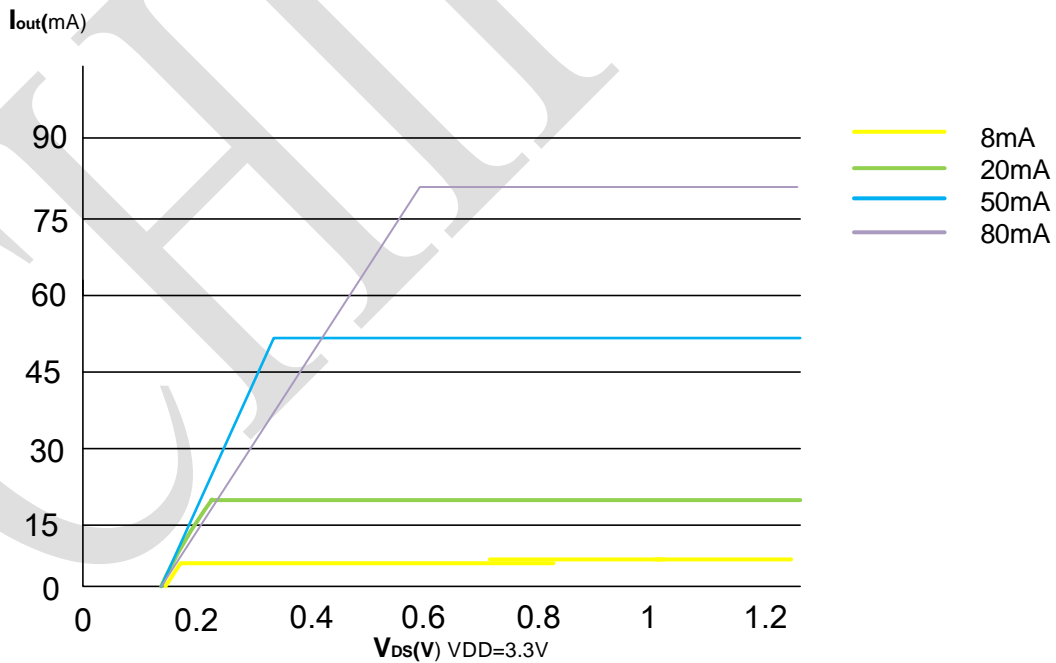
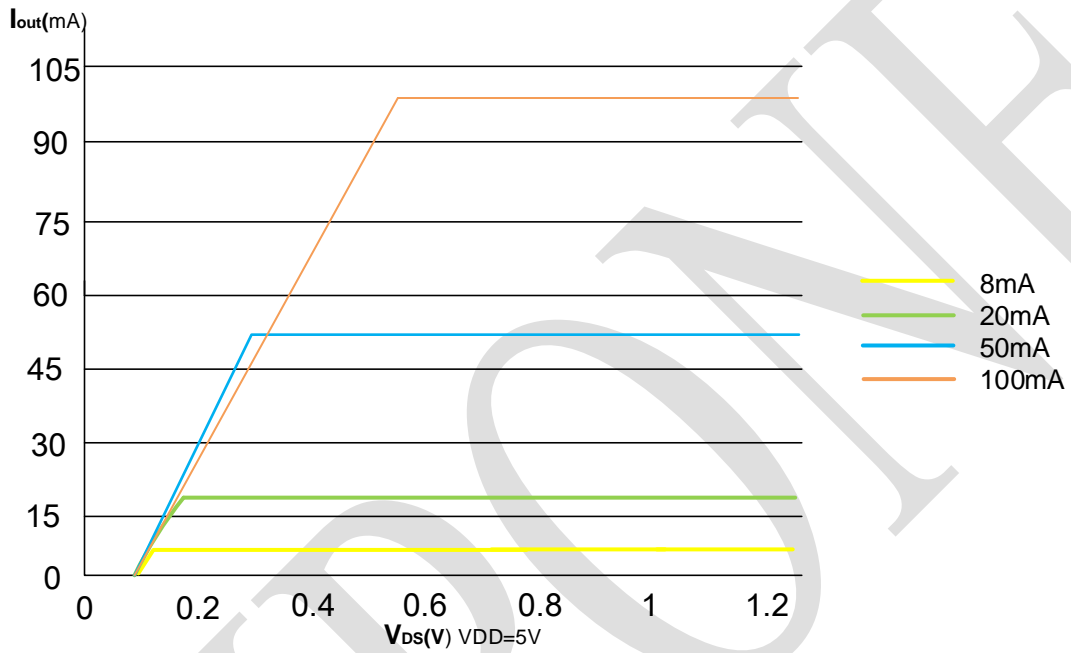
3. $\overline{OUT0}$



Application Information

ICND8390 exploits current precision controlling technology, and provides nearly no current variations from channel to channel and from IC to IC.

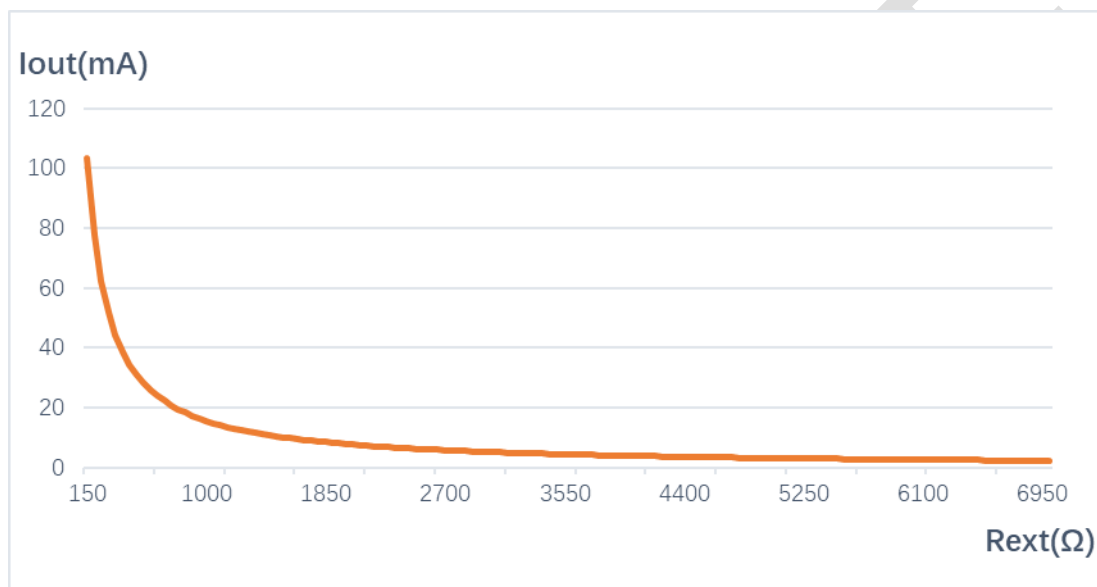
The maximum current variation between channels is less than $\pm 2.0\%$, and that between ICs $< \pm 2.0\%$.



Setting Output Current

The output current (Iout) of ICND8390 is set by an external resistor, Rext. The relationship between Iout and Rext is

$$I_{out} = \text{Gain} * 15.5 / R_{ext} \quad (\text{Gain}=100\%)$$

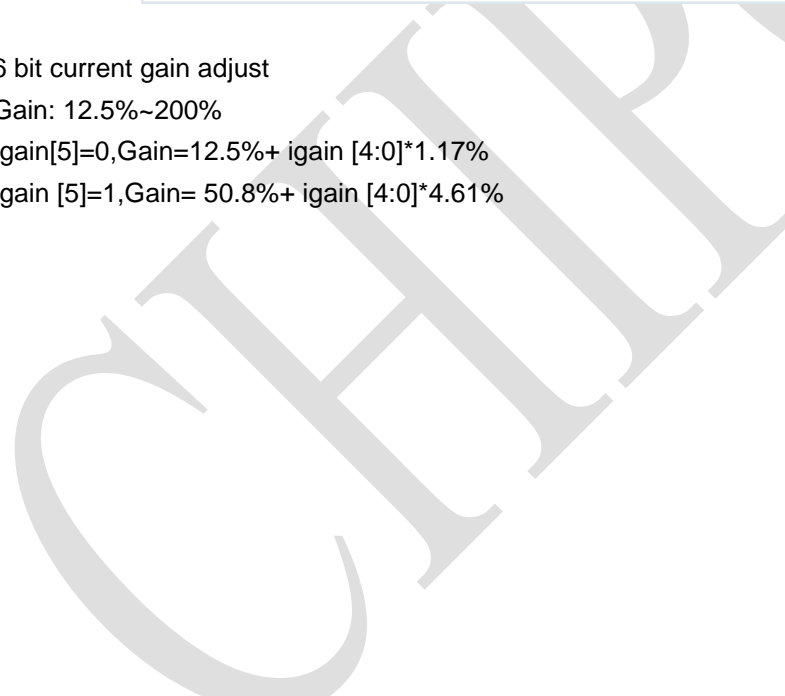


6 bit current gain adjust

Gain: 12.5%~200%

Igain[5]=0, Gain=12.5%+ igain [4:0]*1.17%

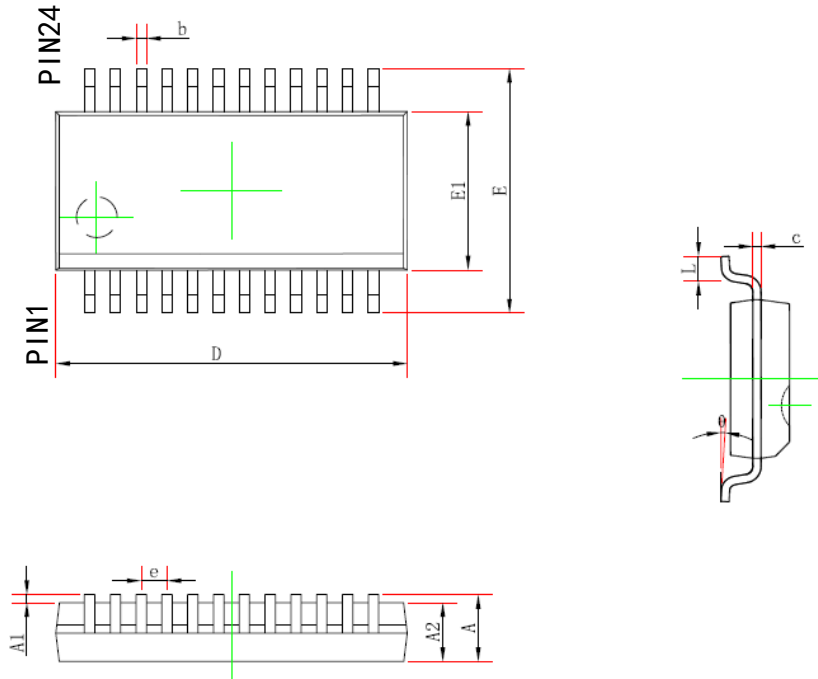
Igain [5]=1, Gain= 50.8%+ igain [4:0]*4.61%



Package Outline

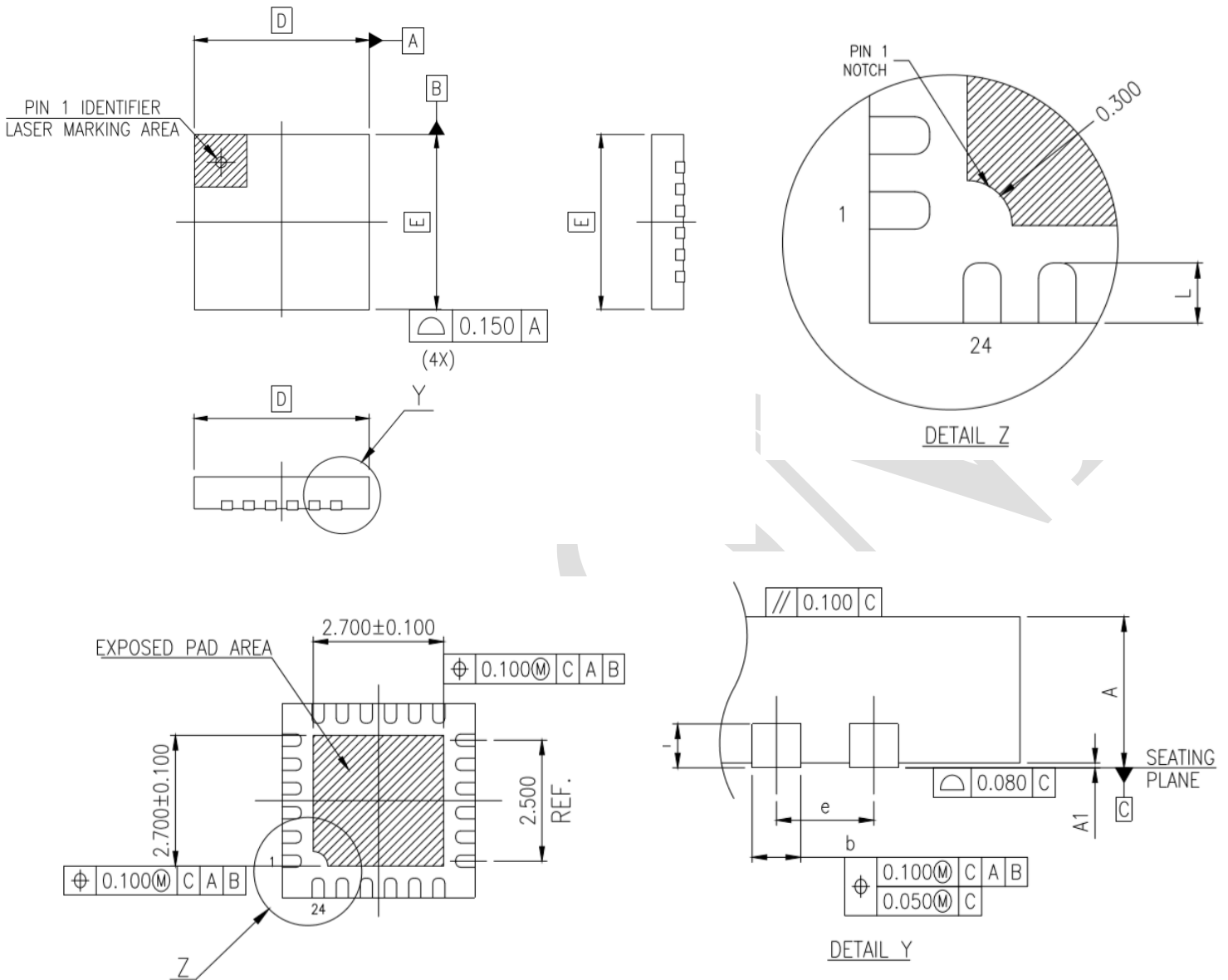
(1) AP:SSOP24-P-150-0.64

SSOP24 (150mil) PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	—	1.750	—	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	—	0.049	—
b	0.203	0.305	0.008	0.012
c	0.102	0.254	0.004	0.010
D	8.450	8.850	0.333	0.348
E1	3.800	4.000	0.150	0.157
E	5.800	6.200	0.228	0.244
e	0.635 (BSC)		0.025 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

(2) AN: QFN24



DIMENSION LIST (FOOTPRINT: 0.80)

S/N	SYM	DIMENSIONS	REMARKS
1	A	0.750±0.050	OVERALL HEIGHT
2	A1	0.020 ^{+0.030} / _{-0.020}	STANDOFF
3	D	4.000±0.100	PKG. LENGTH
4	E	4.000±0.100	PKG. WIDTH
5	L	0.400±0.100	FOOT LENGTH
6	T	0.203±0.008	FRAME THICKNESS
7	b	0.250±0.050	LEAD WIDTH
8	e	0.500 BASE	LEAD PITCH

Product Ordering Information

Product number	Package (Pb-Free)	Weight (mg)
ICND8390AP	SSOP24-P-150-0.635	130
ICND8390AN	QFN24-4*4-0.5	38

Revision History

Rev	Date	Description
1.0	2020/12	Initial Release
1.1	2020/12	Add QFN Package
1.2	2021/01	Add PIN1 on Package Outline
1.3	2021/04	Add Block Diagram
1.4	2021/04	Add V_{DS} Application Information

Important information

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